General Disclaimer

One or more of the Following Statements may affect this Document

- This document has been reproduced from the best copy furnished by the organizational source. It is being released in the interest of making available as much information as possible.

- This document may contain data, which exceeds the sheet parameters. It was furnished in this condition by the organizational source and is the best copy available.

- This document may contain tone-on-tone or color graphs, charts and/or pictures, which have been reproduced in black and white.

- This document is paginated as submitted by the original source.

- Portions of this document are not fully legible due to the historical nature of some of the material. However, it is the best reproduction available from the original submission.

N.I.

BORG-WARNER CONTROLS

DIVISION OF BORG-WARNER CORPORATION
SANTA ANA · CALIFORNIA · 92702

BORG WARNER®

FINAL REPORT FOR

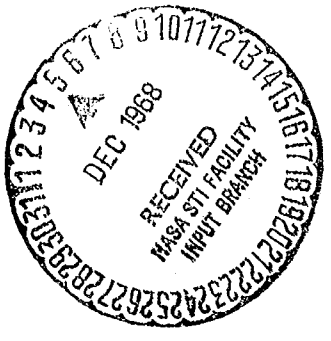
SERVO CONTROL

AND

DATA SYNCHRONIZATION STUDY

REPORT NO. 70-007-F2

UNCLASSIFIED



24 September 1968

Prepared by: Benton Bejach

Benton Bejach
Staff Engineer

Edited by: William Vaughn

William Vaughn
Technical Editor

Approved by: John E. Coolidge

John E. Coolidge
Vice President, Engineering

JPL Contract No. 951659, Final Report.

This work was performed for the Jet Propulsion Laboratory, California Institute of Technology, sponsored by the National Aeronautics and Space Administration under Contract NAS7-100.

BORG-WARNER CONTROLS
DIVISION OF BORG-WARNER CORPORATION
3300 SOUTH HALLADAY STREET
SANTA ANA, CALIFORNIA

NOTICE

This report was prepared as an account of Government-sponsored work. Neither the United States, nor the National Aeronautics and Space Administration (NASA), nor any person acting on behalf of NASA:

a. Makes warranty or representation, expressed or implied, with respect to the accuracy, completeness, or usefulness of the information contained in this report, or that the use of any information, apparatus, method, or process disclosed in this report may not infringe privately-owned rights; or

b. Assumes any liabilities with respect to the use of, or for damages resulting from the use of any information, apparatus, method, or process disclosed in this report.

As used above, "person acting on behalf of NASA" includes any employee or contractor of NASA, or employee of such contractor, to the extent that such employee or contractor of NASA, or employee of such contractor prepares, disseminates, or provides access to, any information pursuant to his employment with such contractor.

Requests for copies of this report should be referred to:

National Aeronautics and Space Administration
Office of Scientific and Technical Information
Washington 25, D.C.
Attention: AFSS-A

No new technology has been discovered to date of this report as a result of this study.

ABSTRACT

The objective of the study was to investigate the feasibility of producing a magnetic tape recorder-reproducer with three distinct capabilities: accepting data pulses at varying rates, making maximum usage of storage space by recording data at a constant packing density, and retrieving the recorded data at a rate synchronized to an external clock.

For digital recording on magnetic tape, maximum usage of data storage is obtained when the data rate is constant. Specialized equipment has been used to achieve a constant recording density, even during periods of varying data rates. Such equipment changes the tape speed to equalize the desired recording rate with the incoming data rate. Because tape speed cannot be changed instantaneously to match a date rate change, a buffer storage system has been used between the data input and the recording head.

Tape speed changes are controlled by a closed-loop electromechanical servo system. Error signal for the servo is derived from the incoming data rate and the amount of data in the buffer storage. Tape speed is adjusted so that gaps are not recorded on the tape and so that incoming data never overflows the buffer storage's capacity.

For data retrieval, the process is somewhat reversed. Data are read from the tape into the buffer storage. Data output from the buffer storage is synchronized to a master clock. The tape speed is then derived from the requirements of the data output rate and from the amount of data in buffer storage.

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS

1.0 INTRODUCTION

The purpose of this report is to present the findings of the Servo Control and Data Synchronization Study. The study was conducted by BWC for Jet Propulsion Laboratory, California Institute of Technology, under JPL Contract 951659, as sponsored by the National Aeronautics and Space Administration under Contract NAS7-100.

This report presents the study's findings by individually describing each segment of the developed system and how that segment functions with reference to other segments. The report also includes such standard considerations as tests, future work areas, conclusions, and new technology. Additionally, all drawings relative to the system have been included to aid the reader's understanding of the system and its individual circuits.

2.0 SERVO AND ASSOCIATED CIRCUITRY

2.1 DEJITTERING (DATA BUFFER)

The schematics S-7841, S-7843, S-7474, and S-8103 pertain to the BWC dejittering, or Data Buffer subsystem. This Data Buffer subsystem consists of three major elements, as shown in block diagram S-7474 and as listed below.

1. The Buffer Register (four, 16 bit I.C. shift registers)
2. Inputting and outputting logic for the Buffer Register
3. Dual Ripple Counters

Also shown in S-7474 is a dual D/A Converter which is used in the servo system but is driven by the Ripple Counters.

The three elements are also shown schematically on drawing S-7843. Each of the elements is separately shown on individual schematics. The Ripple Counters are schematically represented on drawing S-8098. Drawing S-8103 represents the Buffer Register and most of the inputting and outputting logic. The balance of the outputting logic (called gate flip-flop) is represented on S-8108. All cards for the Data Buffer consist entirely of integrated circuits.

The Data Buffer subsystem was exhaustively described in Quarterly Progress Report number 70-007-Q1. For this final report, its operation is summarized as follows.

NOTE

Because the title "Buffer Register" technically applied to the specific buffer register circuit and had been applied as the nomenclature for the subsystem of which it is a member, the subsystem nomenclature has been changed from "Buffer Register" to "Data Buffer". In past reports, references to the Buffer Register should be read as the Data Buffer.

2.1 DEJITTERING (DATA BUFFER) (Continued)

The Data Buffer provides 64 bits of temporary data storage for the serial data tape recorder system during either the record or reproduce modes of operation. The circuitry has essentially three inputs and one output. The two synchronous inputs (inphase and bit rate) are the input data and input clock. In the record mode these two inputs originate from circuits external to the recorder's electronics. The third input signal is called the output clock, and in the record mode it originates from the capstan tape drive digital tachometer. The single output is the data output. The signal from the data output is processed by the Record Amplifier and recorded on the tape. The output clock and output data signals are synchronous inphase and bit rate. The input and output clocks become synchronous in bit rate by the action of the electromechanical capstan servo system. This means that their long term average bit rates are identical. However, in the record mode the input and output clocks (and input and output data signals) may become asynchronous in the bit rate sense, yet remain synchronized inphase. This can occur since the usual definition of "synchronous" implies a one-to-one correspondence between bits of the two clocks, whereas with the Data Buffer subsystem, only the long term average bit rate of the two clocks (and data pulse trains) must coincide. An analogy of a mechanical analog system could consider two cars on a highway which always keep within a fixed distance of each other. One would proceed at a steady rate while the other could accelerate and decelerate violently with accompanying large velocity variations, yet, would always remain within a finite fixed distance of the first car.

The BWC Data Buffer is 50% efficient. Of the four, 16 bit shift register capacity, 32 bits are available for storage; the remaining 32 bits are rendered unavailable, since the register cannot simultaneously have data clocked into it while data is clocked out. Since the Data Buffer is normally operated symmetrically, ± 16 bits of storage are normally available. The Data Buffer requires a NRZL data format, which is transformed from the JPL RZ data format before it reaches the Data Buffer.

Inputs and the output of the Data Buffer are completely different in the reproduce mode. Input clock and input data

2.1 DEJITTERING (DATA BUFFER) (Continued)

are derived from the tape reproduce electronics system. The third input is the output clock, which is supplied externally from the recorder. The output data is the Data Buffer's output. It is synchronous inphase and bit rate with the output clock, hence "dejittered" is the appropriate adjective for this signal.

2.2 D/A CONVERTER

2.2.1 Phase Comparator (Wide Dynamic Range Quantized Output Phase Comparator)

Previous dejittering systems built at BWC provide an output to a capstan servo system which permits the tape signal to be synchronized with an external reference oscillator. For this contract, the dejittering system that was to provide the input to the servo system had to be redesigned to account for the substitution of an ac for a dc motor. The discussion that follows is restricted to a description of that portion of the dejittering system that was redesigned to provide an improved input for the servo system.

The Buffer Register built for this contract is shown on schematic S-7843. The two ÷ 64 counters shown on this schematic provide the inputs to the Digital-to-Analog (D/A) Converter, shown on schematic S-7842. The D/A Converter is synchronized as shown in figure 1.

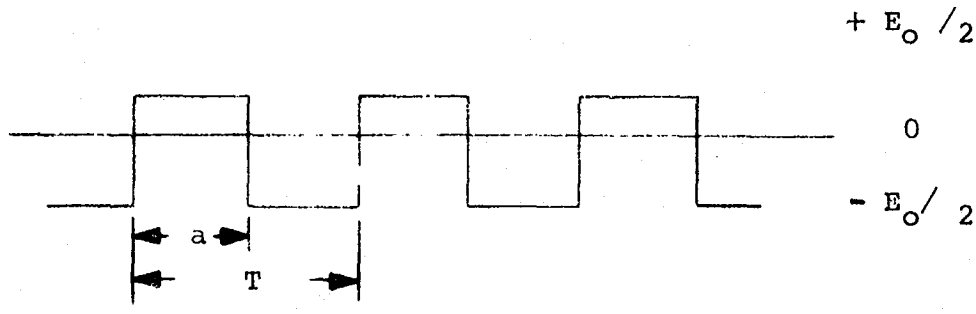


Figure 1. D/A Converter Synchronization

2.2.1 Phase Comparator (Wide Dynamic Range Quantized Output Phase Comparator) (Continued)

The period T of this waveform is the period of the input bit rate, multiplied by the modulus of the counter, in this case 64. The duty cycle of the rectangular wave is represented by the letter a, which can vary from 0 to T (0 to 100%).

When the bit rate is low, such as 300 BPS as specified in the JPL/BWC contract, the period of the D/A Converter's rectangular wave is $\frac{1}{300}$ x 64 second $\cong$ 210,000 microseconds and its frequency is less than 5 BPS. The average value of the D/A Converter's summed output is always zero (see figure 2).

In order to provide an analog output proportional to phase (i.e. to operate properly), the additional circuit element shown in S-7558 was added to the D/A Converter. This element is a simple set-reset flip-flop phased to "hum buck" the $\backsim$ 5 BPS ripple shown in figure 2C. The flip-flop is driven by the MSB (most significant bit) of each Ripple Counter (S-8098). Considered separately, its output's waveform is a square wave of the form shown in figure 3.

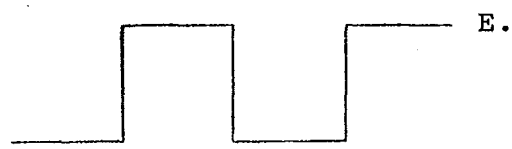


Figure 3. Flip-Flop Output Waveform

When the waveforms of figures 3 and 1, or 2C, are appropriately summed, the resulting waveform is constant, producing a constant phase relationship between the waveforms of figures 2A and 2B. As the phase varies, the summed output varies in proportion with an average delay of T/2 (where T is the period of the input bit rate), which is the same as any sampled data system. Two advantages of this circuit are listed below.

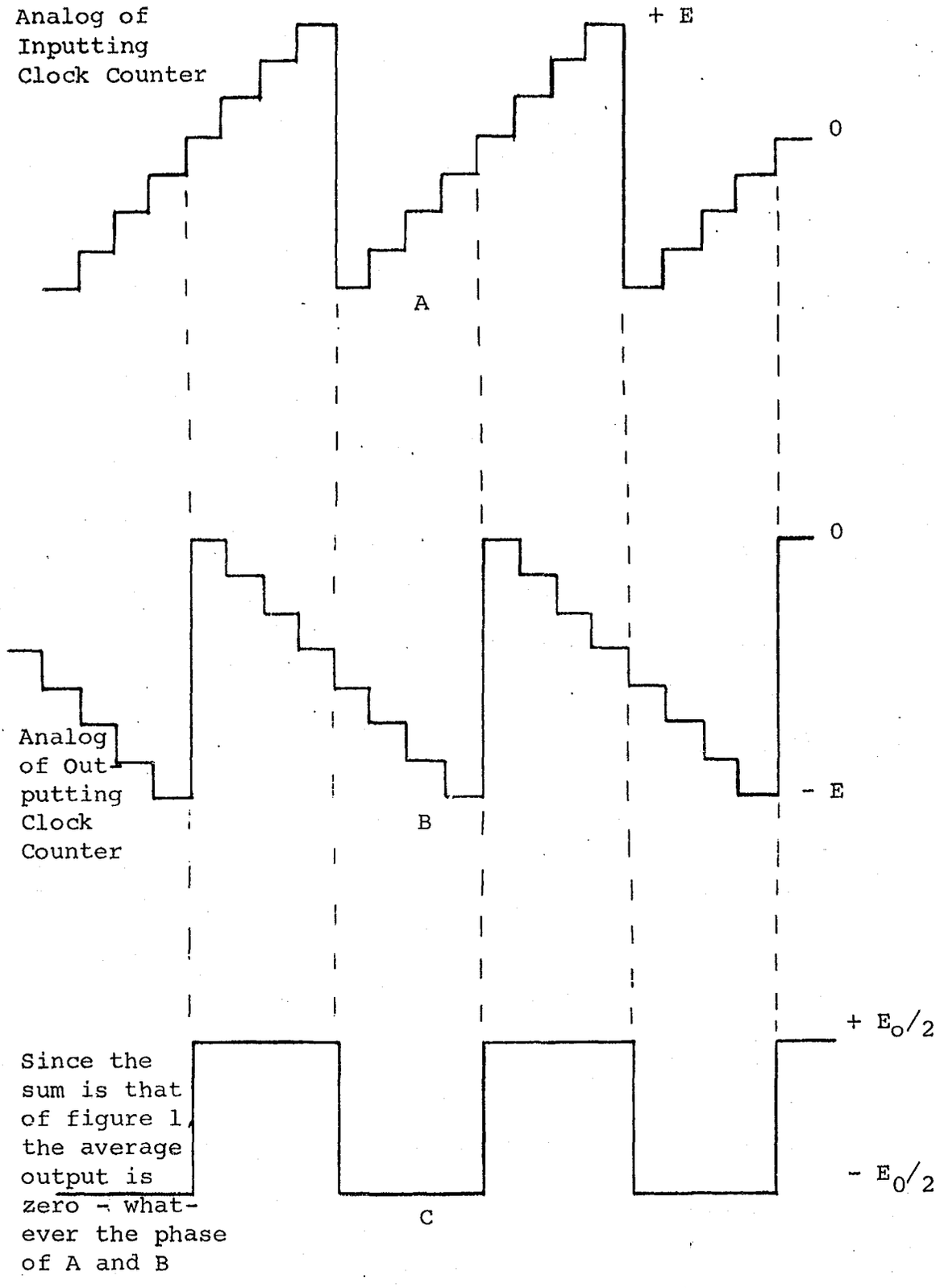


Figure 2.

D/C Converter Summed Output

2.2.1 Phase Comparator (Wide Dynamic Range Quantized Output Phase Comparator) (Continued)

1. The dynamic range is increased by a factor of 64, as applied to this contract. It is this large dynamic range which permits synchronization to be maintained during large increasing steps of the input frequency.

2. The output of the circuit is quantized at the input data rate but with the same number of states as the factor by which the dynamic range is increased. In this case 64 quantization levels are provided. For this and many applications, this degree of quantization is virtually as useful as a continuous analog voltage of the phase comparison and has the added advantage of not requiring ripple filtering. Since ripple filtering inevitably produces phase lag and some signal attenuation, improved fidelity of phase angle measurement is provided by this circuit. Since a larger, more stable bandwidth can be provided with this Phase Comparator than is available when using a conventional single flip-flop, phase comparator and four pole ripple filter, performance of the digital servo systems is improved.

The block diagram for the servo system is shown as part of S-7841, which is the block diagram for the complete system. A simplified version is shown in figure 3 of Quarterly Progress Report 70-007-Q2. The servo block diagram for the system is presented in Appendix A.

2.2.2 Expanded Range Comparator

Schematic S-7842 describes the dual D/A Converter. The drawing is reasonably self-explanatory, showing the interconnections to the Ripple Counters from the inputting and outputting clock signals. Since it was undesirable to have to change connections to terminals 1B through 6B, and 7B through 12B, when it was necessary to make a transfer from the record mode to the reproduce mode, these connections were permanently made. It was then necessary, in order to always provide negative feedback, to invert the output of either Z101 or Z103 through the inverter stage, Z102, selectively; for this purpose relay K3 is used. In either case, the output of Z102 is mixed with the non-inverted

2.2.2 Expanded Range Comparator (Continued)

output from either Z101 or Z103 in mixing amplifier Z104. The third signal, the hum-bucking input (pin 6Z), is also mixed in Z104. It is this connection that permits relatively high frequency signals to be demodulated.

Schematic S-8108 shows the schematic of hum-bucking flip-flop Z102. Potentiometer R103, the circuit's mixing resistor, is used as a one time adjustment that provides for an optimum effect of this circuit. The balance of the schematic is the earlier mentioned partial outputting logic of the Data Buffer and is built on this circuit's card for physical convenience only.

2.3 FEEDBACK AND FEED-FORWARD DISCRIMINATORS

The circuits referenced in this paragraph are shown on drawings S-8073 and S-7839. The circuits are virtually identical and consist of two, dual transistor one-shots, driving two transistor buffer circuits. Potentiometer R108 in each schematic is a gain adjusting potentiometer which varies the output voltage of the circuit. The schematics differ primarily in that the output of the Feed-Forward Discriminator is inverted in comparison to the output from the Feedback Discriminator. The theory of the use of a one-shot as a frequency discriminator is described in Appendix A.

2.3.1 Feedback Discriminator

The function of the Feedback Discriminator is to take the pulses generated by the tachometer, mounted on the capstan motor shaft of the tape transport, and generate an average output voltage proportional to the frequency. The Feedback Discriminator is connected so that when pulses are not received, the output voltage is high; this is the essential source of the negative feedback required for stable servo operation. Because the output voltage is high, full voltage is applied to the dc amplifier, which drives the inverter and, in turn, drives the capstan motor. If too many pulses are received, the average voltage from the Feedback Discriminator approaches a very low value which turns off the dc power supply inverter, causing

2.3.1 Feedback Discriminator (Continued)

the motor to slow down. At the correct operating point, determined by a reference voltage, the frequency discriminator will establish a stable operating point. The theory for this inner-loop, or velocity loop servo system, is described in Appendix A.

Integrated circuit gate Z101 is used with the Feedback Discriminator to shape the pulse from the Pulse Doubler, needed to provide the proper voltage level input to the Ripple Counter. Thus, this feedback circuit is a signal conditioner required between the Pulse Doubler and the Ripple Counter.

2.3.2 Feed-Forward Discriminator

The use of the Feed-Forward Discriminator permits a frequency reference to be used instead of a voltage reference. This second discriminator does not invert its output. Its average output voltage is directly proportional to the input frequency. A calibration curve of the coarse speed control system is shown in figure 4. The purpose of this curve is to show how closely the motion of the tape transport can be controlled by frequency mode control alone. The primary function of these frequency discriminators is to ensure that the system is operating at approximately the correct speed, which prevents any false mode operation (i.e. improper operation at the feedback frequency of double the reference frequency) of the Phase Comparator used in this system.

2.4 TACHOMETER SIGNAL AMPLIFIER AND LIMITING AMPLIFIER

The next schematic to be described is S-7844, which contains a two transistor linear amplifier and two stages of limiting amplifiers. Input to the amplifier is derived from the magnetic tachometer pickup shown in figures 4 and 5 of Quarterly Progress Report 70-007-Q2. The output of such magnetic pickups is directly proportional to both speed and frequency. The greatest gain is at low frequency. This amplifier contains an integrating capacitor C103 which provides a constant output voltage at the linear amplifier, thus preventing clipping which would distort the zero axis crossings of the feedback signal. The signal-to-noise ratio at the amplifier output is a function

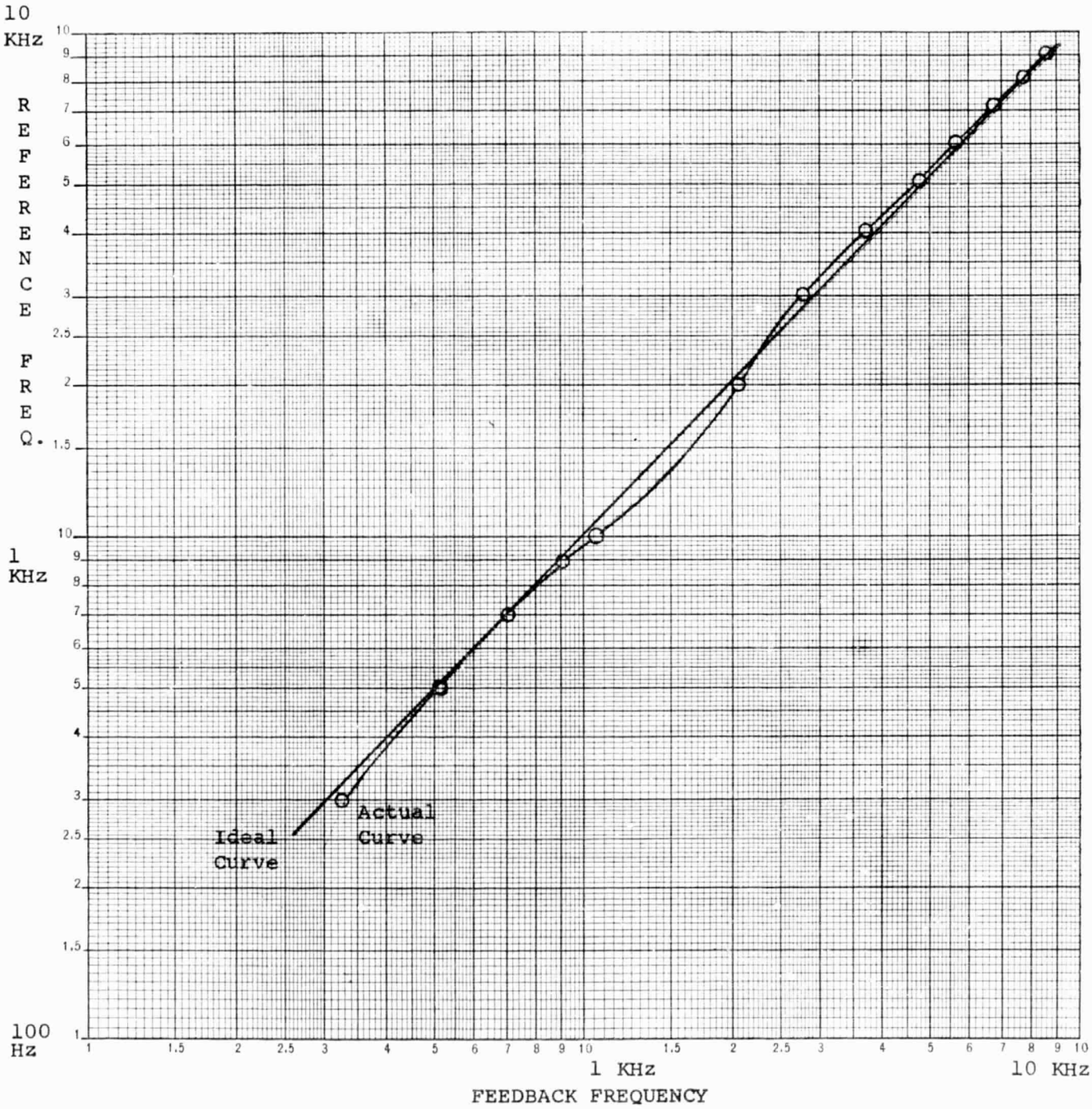


Figure 4. STEADY STATE PERFORMANCE

2.4 TACHOMETER SIGNAL AMPLIFIER AND LIMITING AMPLIFIER (Continued)

of frequency, with less noise present at high frequencies than low frequencies. The primary reason that this system will not operate at a frequency lower than 300 Hz is that the quality of the signal from the magnetic pick-up at such a low speed is considerably degraded. This is one reason that an optical tachometer should be considered for future applications.

The limiting amplifier contains back-to-back feedback diodes which limit the output level at approximately 1.4 volts peak to peak. Two stages of 20 db each are quite adequate for this application.

2.5 PULSE DOUBLER

Schematic S-7840 describes the Pulse Doubler which immediately follows the limiting amplifier in the overall schematic. Pulse doubling is accomplished by using phase splitting transistor Q102, which follows gain stage Q101. Pulses from Q102's collector and emitter are differentiated and positive pulses from each output are then summed at the base of Q103. The latter transistor converts the pulses which are then used to drive the frequency discriminator one-shot circuit (Feedback Discriminator) and, with appropriate signal conditioning, are also used to trigger one of the Ripple Counters in the Data Buffer.

2.6 SIGNAL MIXER AND FOUR POLE FILTER

The circuit of schematic S-7838 performs three functions: amplification, mixing, and filtering. The output from the D/A Converter-Phase Comparator, is amplified by a factor of four by the two transistor amplifier, Q101 and Q102. The amplifier's output is fed into the Four Pole Filter along with the mixed signals from the Feed-Forward and Feedback Discriminators.

Pin 5 of this circuit, labeled as the dc output, can be thought of as the summing point for the four signal voltages used to establish the proper operating point for the servo system. The sources of the four voltages to be summed are listed below:

2.6 SIGNAL MIXER AND FOUR POLE FILTER (Continued)

1. Feed-Forward Discriminator
2. Feedback Discriminator
3. The Amplified D/A Converter-Phase Comparator Output
4. A bias voltage from R109.

Mixing resistors R106, R107, R108, and R109 are used for two purposes: to add the voltages and to provide a means of establishing gain from the four sources. As an example of the latter, if more phase comparator gain is required, the magnitude of R107 should be decreased.

Potentiometer R109, the mixing resistor for the bias voltage, is mounted on the front panel and controlled by a knob so that adjustments can be made as required. By varying the bias voltage setting, the duty cycle of the Phase Comparator is changed; thus the Phase Comparator's duty cycle can be moved to any spot over its large dynamic range by merely adjusting R109.

The Active Four Pole Filter is designed for a 200 Hz corner frequency. Its characteristics are completely described and test results shown in Appendix B. The purpose of this filter is to attenuate the carrier frequency of the servo system so that no significant ripple voltage, which could cause nonlinear operation of the succeeding amplifier, could occur at the carrier frequency. At the same time, the filter must pass the dc output as well as significant low frequency ac components which should also be preserved inphase so that correction of signals may be applied to the succeeding amplifier stage. The reason that the dc output has been isolated and separately provided at pin 5 is that the particular active filter that has been used would ordinarily introduce unnecessary drift into the system. Such dc drift has been completely avoided through the use of the "dc bypass". The ac output at pin 7 is the normal output of the active low pass filter. The signals from the two outputs are recombined at the Passive Filter Servo Preamplifier.

2.7 PASSIVE FILTER SERVO PREAMPLIFIER AND POWER AMPLIFIER

Shown on schematic S-7837 are the phase equalizing filter and dc amplifier used in the servo system. In conjunction with

2.7 PASSIVE FILTER SERVO PREAMPLIFIER AND POWER AMPLIFIER (Continued)

this circuitry a discussion of the signal inverter for the dc amplifier concludes the description of the S-7837 schematic.

The dc and ac outputs from the Active Filter are fed into the dc and ac inputs of this circuit. The ac input is capacitively coupled through pin 8 and capacitor C101. The dc input is resistively coupled through R101. Because of the manner in which components C101 and R101 function, they can be thought of as filter elements. At pin 6 the dc input sees a low pass RC filter; conversely, the ac input at pin 8 sees a high pass RC filter. In each case the low and high pass filters consist of the same components, providing identical time constants. Since the Active Filter and the dc bypass perform their functions of suppressing the ripple and defeating any drift tendency in the Active Filter itself, and since the Passive Filter's time constants are identical, uniform cross-over was achieved.

Transistors Q101 and Q102 comprise a two transistor preamplifier with a dc gain of approximately 40. The preamplifier is diode coupled through CR103 to a similar four transistor power amplifier, consisting of Q103, Q104, Q106, and the externally mounted 2N2151 (connected through pin 10). The Power Amplifier has a gain of approximately 3. Transistor Q105 provides current limiting, sensing the voltage drop across a one ohm resistor in series with the 2N2151 transistor. This Power Amplifier is normally connected directly to a dc, permanent magnet, shunt characteristic motor. However, as an ac motor was used, the Power Amplifier was required to provide a varying voltage to the fixed frequency, 400 Hz, Two-Phase Inverter. The same Power Amplifier was found to be capable of successfully driving the Inverter built to the JPL schematic. Thus the Two-Phase Inverter and the ac motor it drives can be considered as equivalent to the dc motor alone.

The exception to the above statement occurs when deceleration is required. This would be typical of a case when the input frequency would be reduced by a step function of 1,000 Hz. Such a step function would reduce the voltage output of the dc

2.7 PASSIVE FILTER SERVO PREAMPLIFIER AND POWER AMPLIFIER (Continued)

amplifier to zero. Unlike a dc motor drive system, negative voltage cannot be applied to the Inverter, nor is dynamic braking readily available. Schematic S-7881 illustrates a circuit which was developed, at the request of JPL, to permit phase reversal of one of the motor phases, allowing the necessary braking torques to be developed. This circuit contains a threshold potentiometer, R205, which is used to trigger reversing relay K1. Proper execution of this function also requires inversion of the signal through the dc amplifier. This additional circuitry was never implemented, due to low priority in executing this CPFF program. Thus, this circuit is included in the breadboard, but potentiometer R205 is adjusted in such a way that renders the circuit inoperative.

3.0 SERVO SYSTEM OPERATION

The theory of operation of the capstan servo system was previously described in Quarterly Progress Report 70-007-Q1.

Closed loop operation of the servo system was first obtained using the inner loop, or Feed-Forward and Feedback Discriminator, subsystem only. This subsystem is described in Appendix A. At that time it was readily apparent that the nonlinearity in the initial system posed an upper limit on the frequency response of the servo system. The reason that the nonlinearity existed, as discussed fully in Quarterly Report 70-007-Q1, is that the ac motor could not be decelerated as rapidly as it could be accelerated. Similarly, the rise time characteristics for a step upward in frequency indicates that there is an upper limit to the frequency response, due to still another type of nonlinearity. The latter nonlinearity is essentially that of the maximum voltage, 28 Vdc, supplied to the Inverter. The 28 Vdc, converted to the 400 Hz ac voltage and applied to the motor, provides only limited accelerating torque for the motor used in the tape transport supplied by JPL. When the inertia of the tape transport system was significantly increased by the addition of the gear-tooth tachometer disc to the motor shaft (see Quarterly Progress Report 70-007-Q2), it became apparent that a low bandwidth and relatively low dynamic performance servo system would result from the use of the ac motor and inverter system.

4.0 SIGNAL ELECTRONICS

4.1 RECORD AMPLIFIERS

As previously discussed, the inputs to the two Record Amplifiers are derived from the outputs of the Data Buffer and the output clock. In this case, the output clock is the tachometer, mounted on the capstan motor shaft. The integrated circuits, DTL 932 gates, shown on schematic S-7880 are used for record head drivers. The output of the gates is balanced with respect to ground, permitting current reversal in the record heads. Resistors R116 and R117 control the record current. The format of the recorded data on the tape is NRZL.

4.2 REPRODUCE PREAMPLIFIERS

Drawing S-7882 is a schematic for the integrated circuit linear preamplifiers and output buffer transistors. These preamplifiers are low input impedance devices. As specified, at the 1,000 bit per inch packing density, the output waveforms from the tape recorder and the Applied Magnetics Corporation heads have a great deal of inflection and low pulse crowding characteristics.

4.3 DATA AND CLOCK INPUT BUFFERS

Drawing S-8072 shows the interface between the JPL supplied data and clock input lines, pins 3 and 4, and the Data Buffer. The input data format is RZ while the data format from the buffers to the Data Buffer is NRZL.

4.4 PEAK DETECTOR

Drawing S-7877 illustrates the dual Peak Detector which receives the data and clock outputs from the preamplifiers. The clock output is reconstructed as a squarewave while the preamplifier data output is formatted to NRZL, which is necessary for proper operation of the Data Buffer as used in the reproduce mode. Note that the outputs from the Peak Detectors become the input clock and input data to the Data Buffer.

4.5 OUTPUT SIGNAL CONDITIONER

After the dejittered data leaves the Data Buffer it is converted to the RZ format. Data is then ready to be received by JPL equipment.

5.0 INTERCONNECTION DIAGRAMS AND MISCELLANEOUS

Drawing S-8104 is an interconnection diagram between all cards, the power supplies, inputs and outputs, and the cable supplied for use with the tape transport.

5.1 CONTROL SWITCH CARD

Drawing S-8107 shows the mode switching wafer interconnections. This card also contains the reverse relay, used with a manual reversing switch to change the direction of tape movement. In future applications, its coil could be operated by appropriate circuitry so that the end-of-tape sensors would automatically reverse the direction of tape travel.

5.2 MISCELLANEOUS DRAWINGS

Most of the BWC circuitry operates from a regulated 28 volt supply. In order to avoid an extra laboratory power supply, a three transistor, 20 volt regulated supply is provided. Its schematic is on drawing S-7878. The regulated 20 volts is derived from the 28 volt supply which is also used for the capstan motor and inverter power supply. Also shown on this schematic are the end-of-tape sensor amplifiers. Another miscellaneous drawing is S-8105, which shows the cable connections mounted to a vector card.

5.3 MECHANICAL DRAWINGS

BWC does not provide the tape transport, thus a set of mechanical drawings is not required. The only exception to this is a gear tachometer which was installed by BWC as necessary to the completion of this contract. The assembly drawing for the tachometer is S-8101, showing the gear and hub assembly. Each of these items is shown separately in drawings S-8099 and S-8100, respectively. To adapt the tachometer to the shaft of the capstan motor, the spacer shown in S-8106 is required. The spacer prevents interference between the tachometer and the first stage of Mylar* belt reduction. A photograph of the assembly installed on the tape recorder is shown in figure 4 of Quarterly Progress Report 70-007-Q2.

*tradename of E. I. DuPont deNemours & Co.

6.0 TESTS

6.1 TEST RESULTS

Many preliminary tests were conducted during the development of the servo control and data synchronization study. Periodically these tests were repeated for the benefit of JPL personnel. Due to insufficient funding, the full testing program was not performed at the end of the program. Test data include the following significant items:

6.1.1 Servo System Step Function Responses

Servo system step function responses were measured by the expanded dynamic range phase comparator. The responses shown in the photographs of figure 5 are expressed as a function of time over the 30:1 frequency range.

6.1.2 Data Buffer Step Function Responses

Data buffer step function responses were photographed at high, medium, and low bit rates. These responses, illustrated in figure 6, were photographed during the record mode operation.

6.2 CONCLUSIONS DERIVED FROM TEST RESULTS

6.2.1 Servo System

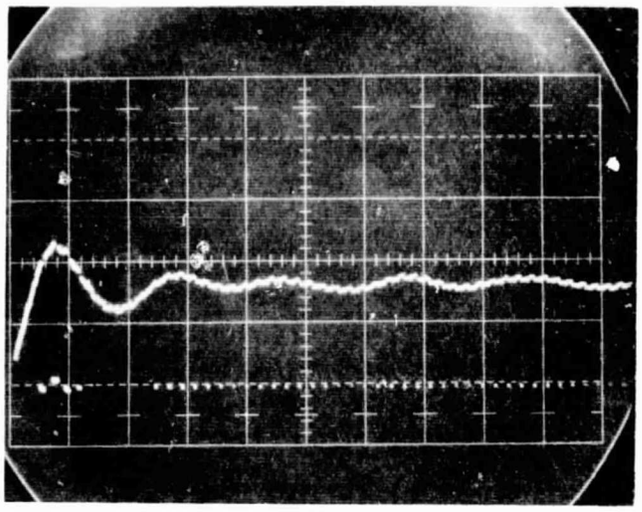
The servo system remains phase locked during upward, but not downward, reference frequency steps of 1,000 Hz.

6.2.2 Data Buffer

The Data Buffer provided proper uninterrupted record data for upward steps of 500 BPS at all frequencies except the low range.

Before shipping the breadboard electronics to JPL, the complete record/reproduce system was tested. Due to noise introduced in the reproduce electronics, fully satisfactory operation of the Data Buffer was observed but with excessive

STEP FREQUENCY 440 Hz to 1454 Hz, Δ 1014 Hz

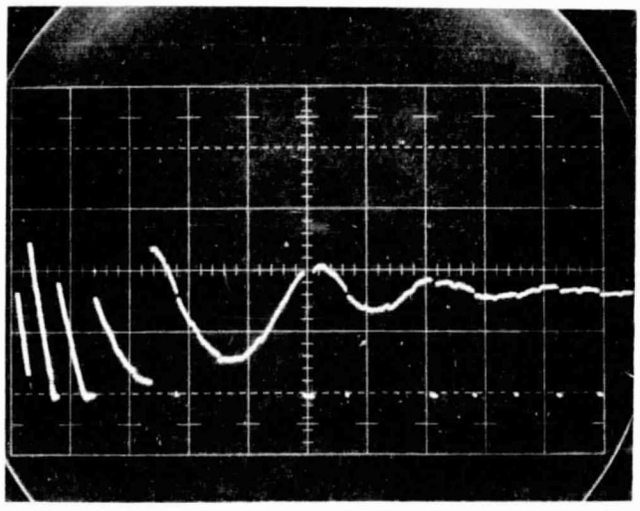


OUTPUT OF D/A CONVERTER (TP4)

Note: Step up in frequency,
440 Hz to 1454 Hz

Horizontal 0.2 sec/cm

Vertical 1 V/cm



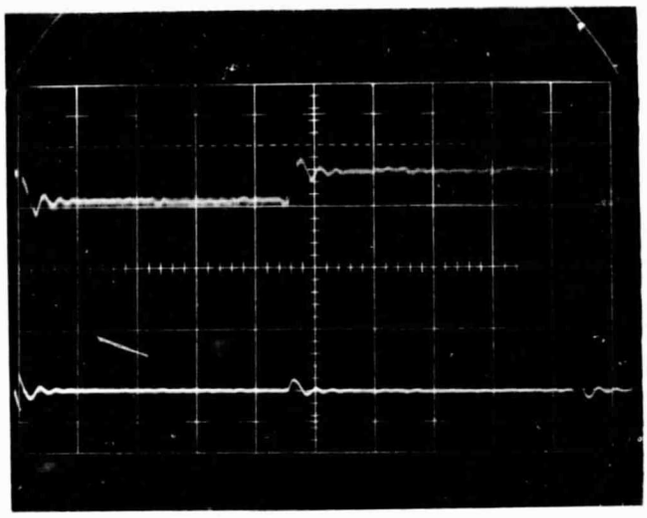
Note: Step down in frequency,
1445 Hz to 440 Hz

Horizontal 0.2 sec/cm

Vertical 1 V/cm

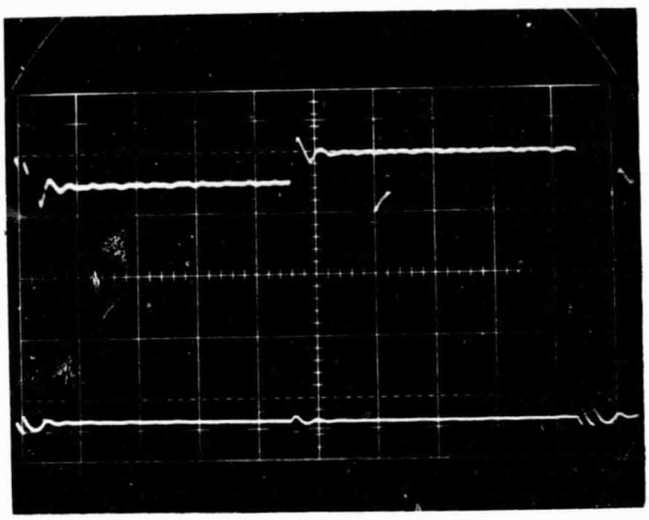
Figure 5.

RECORD STEP RESPONSE



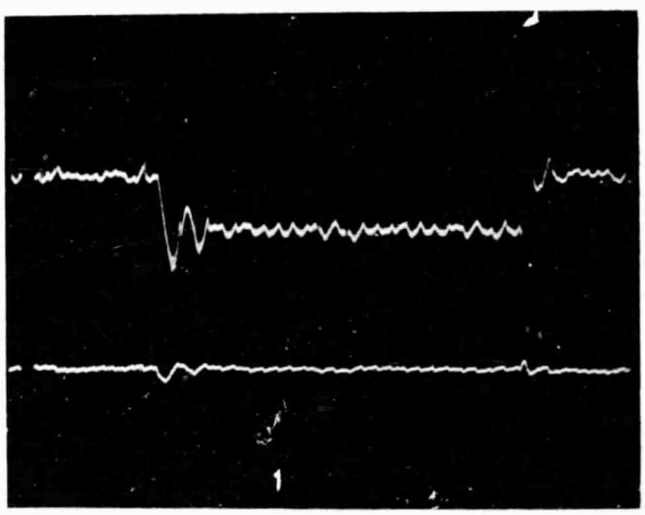
7105 Hz
Data 514 Hz HIGH
6591 Hz

Servo



2171 Hz
Data 512 Hz MEDIUM
1659 Hz

Servo



496 Hz
Data 155 Hz LOW
341 Hz

Servo

Figure 6.

6.2.2 Data Buffer (Continued)

bit loss, particularly at the lower speeds. BWC feels that these results can be greatly improved by optimizing the reproduce subsystem.

7.0 FUTURE WORK AREAS

To improve the reproduce signal-to-noise, center tapped reproduce heads should be used, which would offer a superior common mode rejection ratio. An improved preamplifier circuit is also recommended.

If higher than 1,000 BPI tape packing density is desired (with the same gap length reproduce head), peak detection may be less satisfactory than the biphase reproduce technique using limiting amplifiers to establish zero axis crossings. To match the servo performance, the Data Buffer capacity should be doubled. This can be implemented by doubling the capacity of the Buffer Register section.

Conversely, a faster responding servo system will permit use of the existing Data Buffer. This can be implemented by operating the motor at a higher voltage and by increasing the power capacity of the inverter. To achieve equivalent slow-down to speed-up servo performance, BWC recommends the use of a conventional ac suppressed carrier double side band modulator and a linear servo power amplifier driving the control phase of the motor winding. Such a system would solve the coordination problem of amplifier inversion and motor control winding with phase angle switching.

Because the presently used magnetic pick-up is incapable of efficient operation at lower frequencies, an optical tachometer should be substituted. Such a tachometer would expand the capabilities of the system and would provide a useful signal from the tachometer at frequencies below 300 Hz.

8.0 CONCLUSION

BWC feels that its servo and Data Buffer designs and schematics are sound and permit achievement of the JPL system requirements. However, the reproduce subsystem is marginal and should be improved.

The first problem that confronted BWC was the implementation of servo and dejittering electronics. The problem was seen not only as of major importance but of primary significance. Consequently, the servo-dejittering problem received the bulk of the engineering effort. Because BWC's experience in record and reproduce electronics is extensive, that portion of the system's electronics was left for development and improvement during the latter period of the program. However, as the close of the study neared, problems with the record and reproduce electronics began to unfold, problems which were not as easily overcome as had been previously anticipated.

9.0 NEW TECHNOLOGY

In the area of new technology, it is the opinion of BWC that the expanded range Phase Comparator used in the servo subsystem represents work that has not been previously documented. The fact that this low bandwidth capstan servo system remains phase locked when a step function of the reference frequency is imposed upon it demonstrates the advantages of the expanded range phase comparator. Without the expanded range, discontinuities occur during very small reference frequency steps, at which time data is irretrievably lost. (Figure 5B shows the presence of such discontinuities on large down steps even when the expanded range phase comparator is used.)

10.0 APPLICABLE DRAWINGS

All drawings associated with the JPL contract are presented in this section. The following is a list of the drawings in the order in which they appear.

S-8102
S-7474
S-7837
S-7838
S-7839
S-7840
S-7841
S-7842
S-7843
S-7844
S-7877
S-7878
S-7880
S-7881
S-7882
S-8072
S-8073
S-8098
S-8099
S-8100
S-8101
S-8103
S-8104
S-8105
S-8106
S-8107
S-8108

A-5-8102

CARD ADDRESS LIST

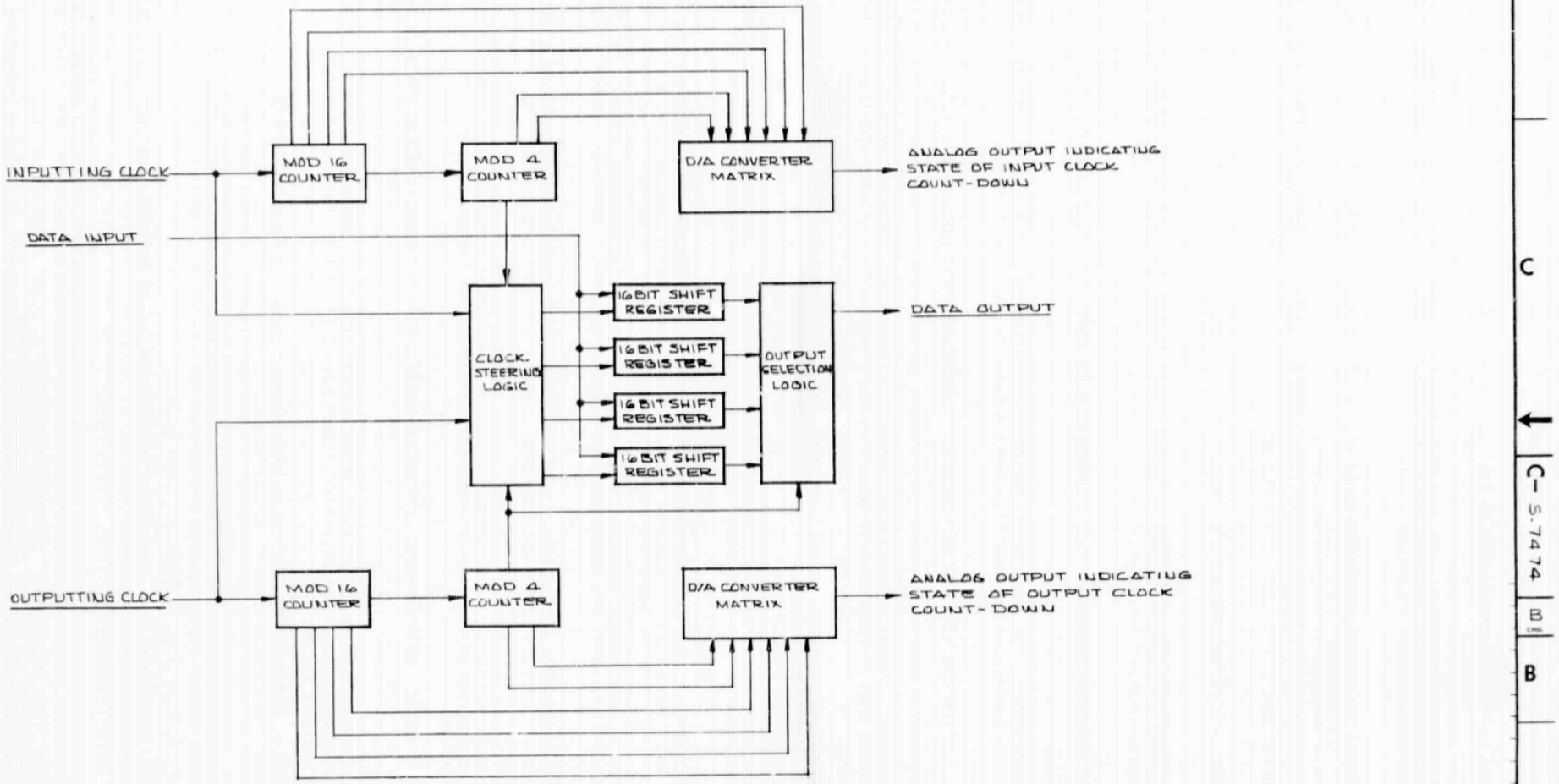
TOP

SERVO POWER AMPLIFIER C-S-7837	D A CONVERTER D-S-7842
SERVO PREAMPLIFIER C-S-7837	
REV RELAY DRIVER B-S-7881 SIG MIXER & 4 P FIL C-S-7838	RIPPLE COUNTERS D-S-8098
FEEDBACK DISCR & GATE C-S-8073	
PULSE DOUBLER C-S-7840	BUFFER REGISTER C-S-8103
TACH AMPL & LIMITER D-S-7844	HUM BUCK & MODE RELAY GATE FLIP FLOPS C-S-8108
20V REG, EOT-BOT SENSORS C-S-7878	FEED FORWARD DISCR C-S-7839
CONTROL SWITCH C-S-8107	DATA & CLOCK RECORD C-S-7880
	DATA & CLOCK PREAMPL C-S-7882
CARD 4* 400 CY INV MOTOR DRIVER ϕ A	DATA & CLOCK PEAK DET C-S-7877
CARD 3* 400 CY INV MOTOR DRIVER ϕ B	SPARE
CARD 2* 400 CY INV GATING	DATA - CLOCK INPUT BUFFERS C-S-8072
CARD 1* 400 CY INV OSC & DIVIDER	DATA - CLOCK INPUT & OUTPUT CABLES B-S-8105

* SEE JPL DWG C-J4210052

CARD NUMBERS REFER TO SCHEMATIC NOS.

REVISIONS						
CHG.	ZONE	DESCRIPTION	E.C.O.	DATE	BY	CHKD
A		REVISED TITLE	—	7/15	GE	
B		REVISED CLOCK INPUT & OUTPUT NOMENCLATURE	—	8/18	GE	



ITEM	REQ'D	PART NO.	DESCRIPTION	MATERIAL	SPEC.	NOTE	SYMBOL
		S/O 76094-01	LIST OF MATERIALS				

NEXT ASSY. | USED ON | PARTS LIST NO.
APPLICATION

SPECIFICATIONS UNLESS OTHERWISE NOTED
ALL DIMENSIONS APPLY BEFORE ADDITIVE FINISH
BREAK ALL EDGES AND SHARP CORNERS [ ] MAX.
SURFACE ROUGHNESS √ MICRO INCH R.M.S. MAX.
DIAMETERS TO BE CONCENTRIC WITHIN [ ] T.I.R.
FILLET RADIUS [ ] MAX.

DRAWN BY	G. EVALLS	DATE 1-31-67
CHECKED BY	[illegible]	DATE 4-6-68
DESIGN APP.	[illegible]	DATE
PROJ. ENGR.	B. Bogacki	DATE 2-1-67

MATERIAL —
HEAT TREATMENT —
PROTECTIVE FINISH —

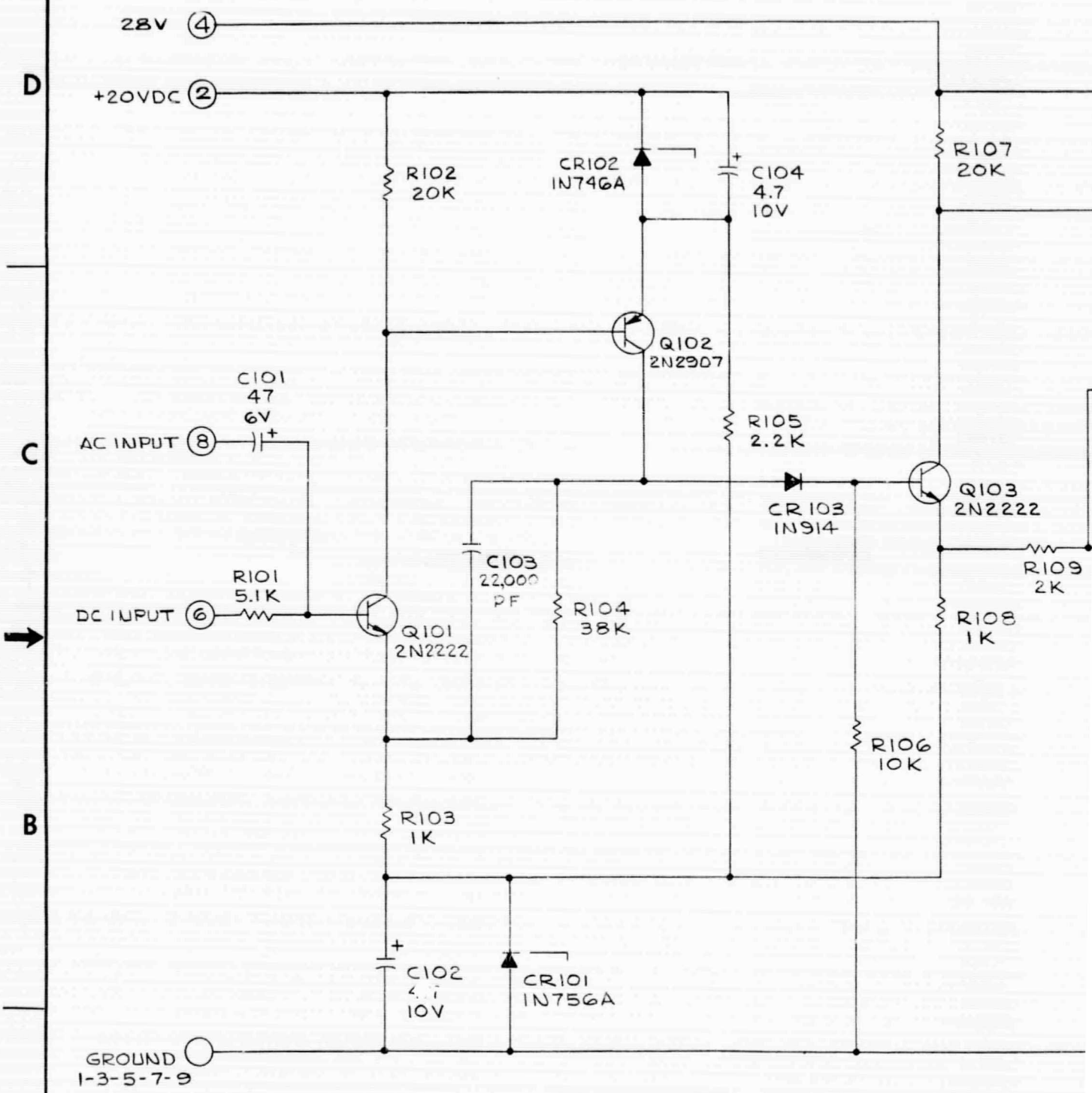
DATA BUFFER BLOCK DIAGRAM

SCALE — DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS —
ANGLES — FRACTIONS —

BORG-WARNER CONTROLS
3300 SO. HALLADAY STREET
SANTA ANA, CALIFORNIA

DWG. C S-7474 CHG. B

C- S-7474 B (CHG.)



2. CAPACITOR VALUES ARE IN MICROFARADS ±10%.

1. RESISTOR VALUES ARE IN OHMS, ±5%, 1/4 W.

NOTES: UNLESS OTHERWISE SPECIFIED.

ITEM	REQ'D	PART NO.
		S/O 76094

SPECIFICATIONS UNLESS OTHERWISE NOTED

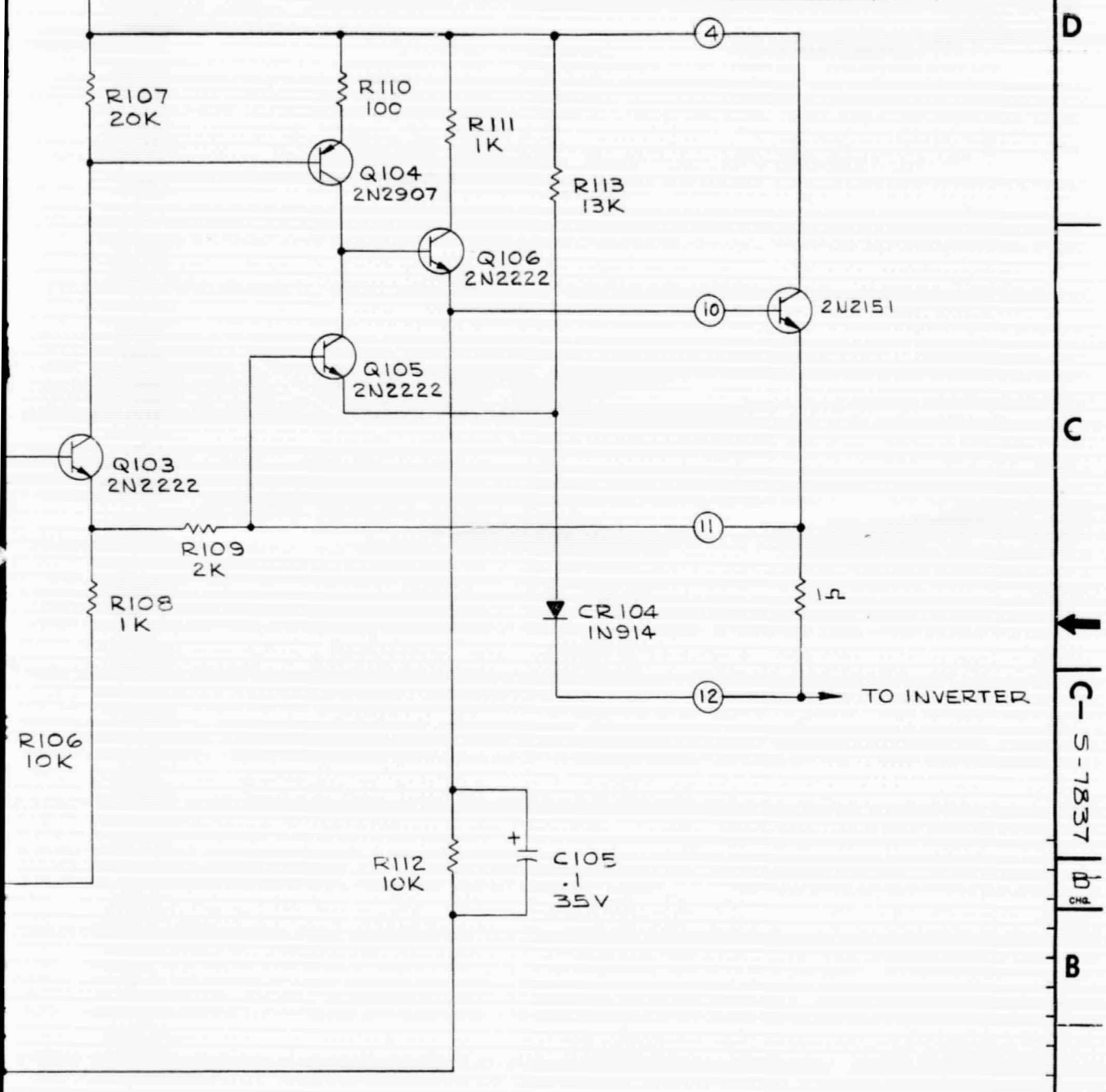
ALL DIMENSIONS APPLY BEFORE ADDITIVE FINISH
BREAK ALL EDGES AND SHARP CORNERS [ ] MAX.
SURFACE ROUGHNESS ✓ MICRO INCH R.M.S. MAX.
DIAMETERS TO BE CONCENTRIC WITHIN [ ] T.I.R.
FILLET RADIUS [ ] MAX.

DRAWN BY W. SOUTAR	DATE	8-16-67
CHECKED BY	DATE	4-8-68
DESIGN APP.	DATE	4-8-68
PROJ. ENGR.	DATE	

NEXT ASSY.	USED ON	PARTS LIST NO.
	APPLICATION	

FOLDOUT FRAME 1

REVISIONS						
CHG.	ZONE	DESCRIPTION	E. C. O.	DATE	BY	CHKD
A		DELETED CKT BETWEEN C104 & R107 ADDED 2N2151 & 1Ω RESC	—	9/5/67	GE	
B		TERM. 2 WAS 1; Q102 WAS 2N2222; REVISED TITLE	—	3/12/68	GE	V.I E.H.



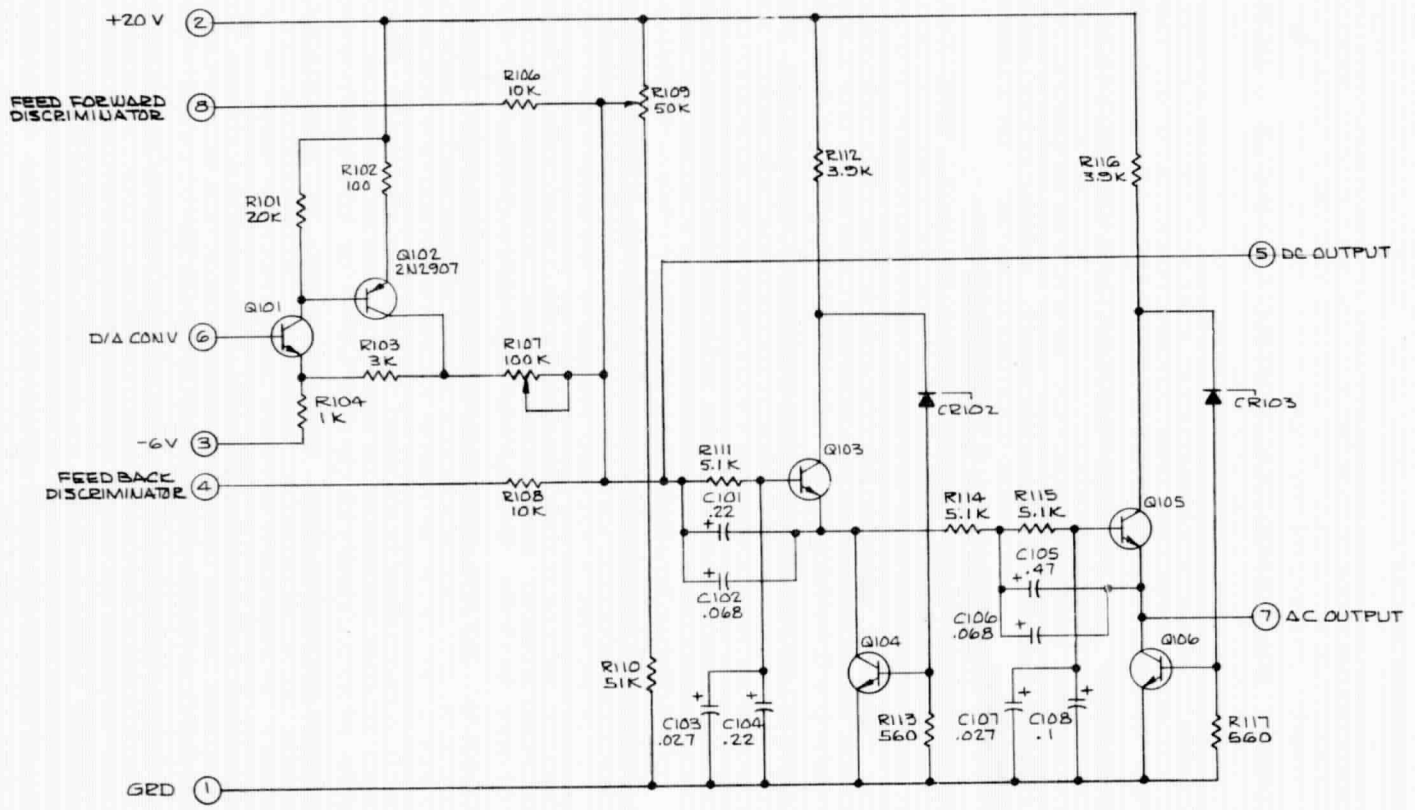
Q'D	PART NO.	DESCRIPTION	MATERIAL	SPEC.	NOTE	SYMBOL
6094						

LIST OF MATERIALS

FICATIONS UNLESS OTHERWISE NOTED	MATERIAL	SCHEMATIC PASSIVE FILTER SERVO PREAMPL & POWER AMPL	BORG-WARNER CONTROLS		
VISIONS APPLY BEFORE ADDITIVE FINISH					
EDGES AND SHARP CORNERS ☐ MAX.	HEAT TREATMENT		3300 SO. HALLADAY STREET SANTA ANA, CALIFORNIA		
OUGHNESS ✓ MICRO INCH R.M.S. MAX.					
TO BE CONCENTRIC WITHIN ☐ T.I.R.					
DIUS ☐ MAX.					
W. SOUTAR DATE 8-16-67	PROTECTIVE FINISH	SCALE ——— DO NOT SCALE DRAWING	DWG. C	S-7837	CHG. B
DATE 4-8-68		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS ——— ANGLES ——— FRACTIONS ———			
DATE 4-8-68					
DATE					

FOLDOUT FRAME 2

REVISIONS						
CHG.	ZONE	DESCRIPTION	E.C.O.	DATE	BY	CHKD
A		REVISED & REDRAWN	—	3/7/68	GE	
B		DELETED R105 & CR101 ADDED TERM. 3	—	3/21/68	GE	VEH.
C		REVISED TERM DESIG.	—	4/16/68	GE	
D		REVISED PLACEMENT OF Q102	—	5/16/68	GE	



5. THIS CIRCUIT IS ON THE SAME CARD AS S-7881
4. TRANSISTORS ARE 2N2222
3. DIODES ARE IN759A
2. CAPACITOR VALUES ARE IN MICROFARADS ±10% 35V
1. RESISTOR VALUES ARE IN OHMS ±5% 1/4 W

NOTES: UNLESS OTHERWISE SPECIFIED

ITEM	REQ'D	PART NO.	DESCRIPTION	MATERIAL	SPEC.	NOTE	SYMBOL
		S10 76094	LIST OF MATERIALS				

SPECIFICATIONS UNLESS OTHERWISE NOTED
ALL DIMENSIONS APPLY BEFORE ADDITIVE FINISH
BREAK ALL EDGES AND SHARP CORNERS — MAX.
SURFACE ROUGHNESS √ MICRO INCH R.M.S. MAX.
DIAMETERS TO BE CONCENTRIC WITHIN — T.I.R.
FILLET RADIUS — MAX.

MATERIAL —
HEAT TREATMENT —
PROTECTIVE FINISH —

DRAWN BY	G. EVANS	DATE 9-19-67
CHECKED BY		DATE 4-5-68
DESIGN APP.		DATE 4-5-68
PROJ. ENGR.		DATE

NEXT ASSY. | USED ON | PARTS LIST NO.
APPLICATION

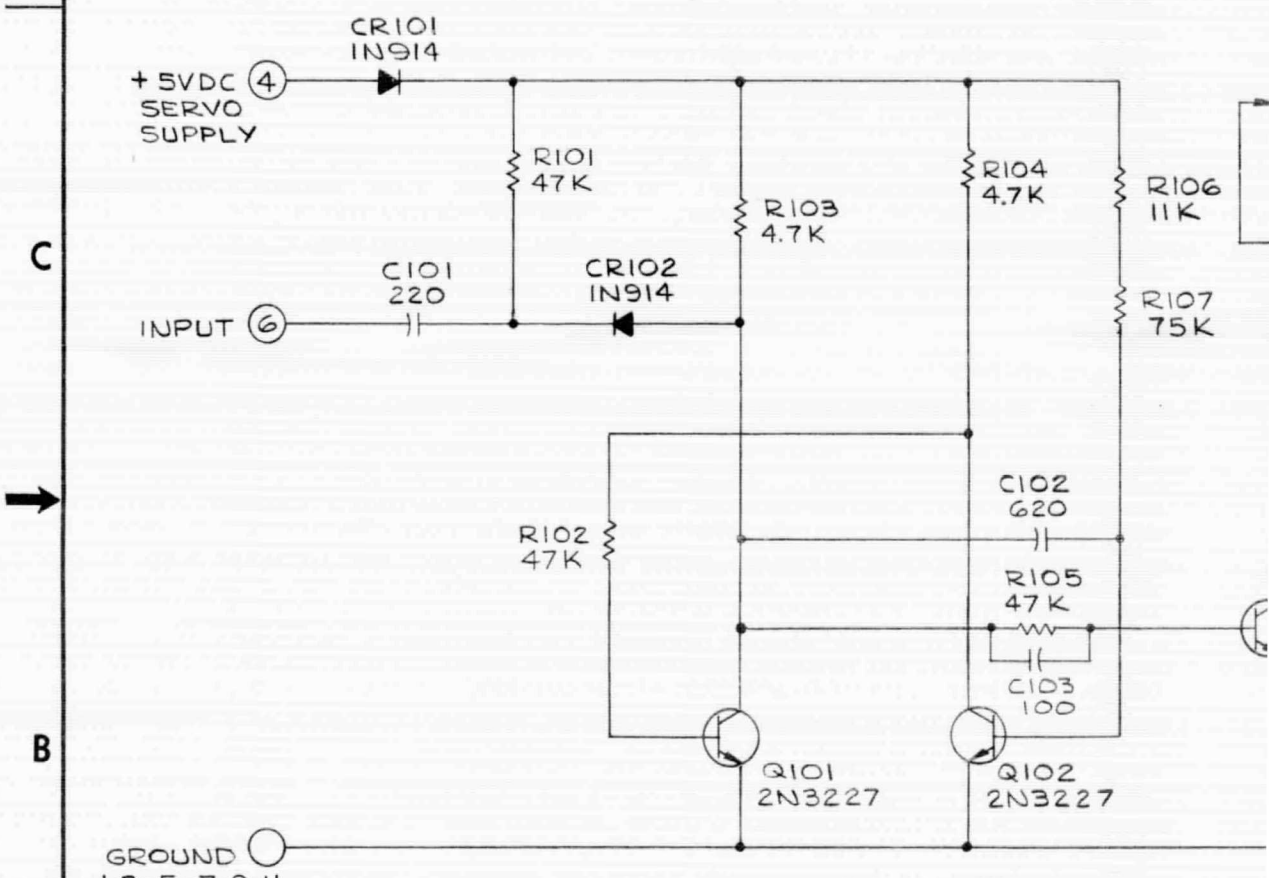
SCHEMATIC SIGUAL MIXER & 4 POLE FILTER

SCALE — DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS —
ANGLES — FRACTIONS —

BORG-WARNER CONTROLS
DIVISION OF BORG-WARNER CORPORATION
3300 SO. HALLADAY STREET
SANTA ANA, CALIFORNIA

DWG. C S-7838 CHG. D

C-S-7838 D CHG.



2. CAPACITOR VALUES ARE IN PICOFARADS, ± 10% 200V

1. RESISTOR VALUES ARE IN OHMS, ± 5%, 1/4 W.

NOTES: UNLESS OTHERWISE SPECIFIED

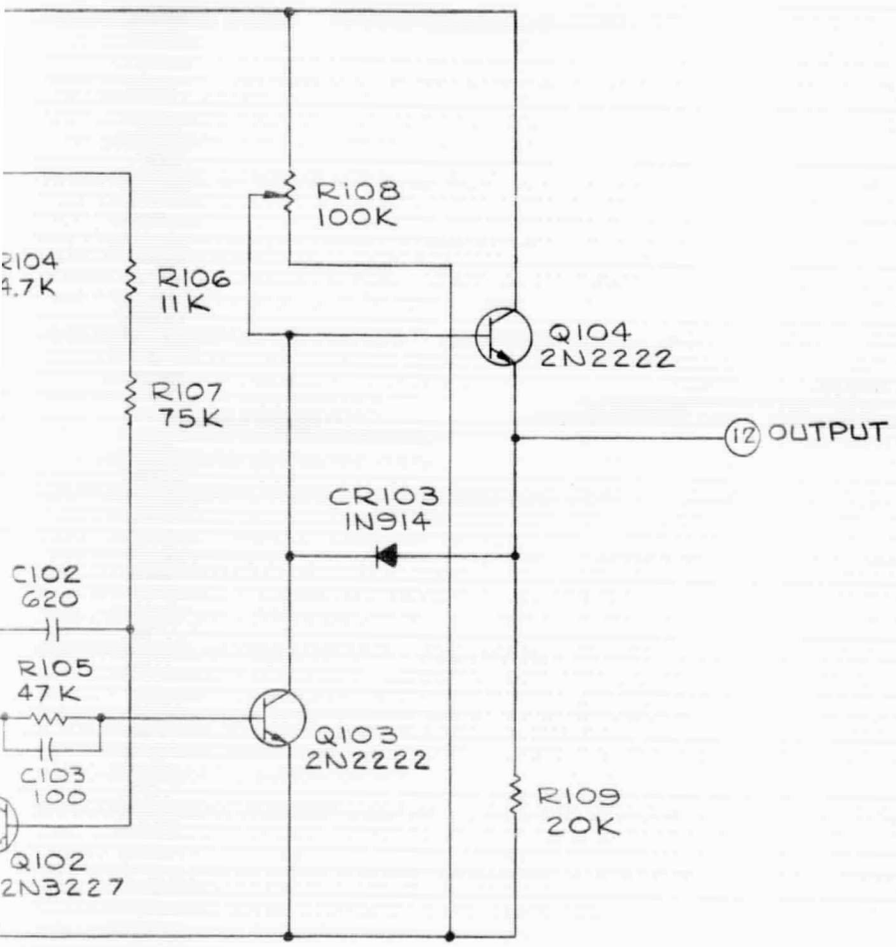
NEXT ASSY.	USED ON	PARTS LIST NO.
	APPLICATION	

ITEM	REQ'D	PART
S/O 76094		

SPECIFICATIONS UNLESS
ALL DIMENSIONS APPLY BE
BREAK ALL EDGES AND SHAR
SURFACE ROUGHNESS √
DIAMETERS TO BE CONCENTR
FILLET RADIUS ☐ MAX.
DRAWN BY W. SOUTAR
CHECKED BY
DESIGN APP
PROJ. ENGR.

FOLDOUT FRAME 1

REVISIONS						
CHG.	ZONE	DESCRIPTION	E. C. O.	DATE	BY	CHKD
A		TERM. 12 WAS 8; NOTE 2 WAS MICROFARADS; R108 WAS CONNECTED TO Q104-B	—	3/12/68	GE	V. E. H.
B		ADDED C103; REV TITLE	—	4/4/68	GE	



ITEM	REQ'D	PART NO.	DESCRIPTION	MATERIAL	SPEC.	NOTE	SYMBOL
S/O 76094			LIST OF MATERIALS				

SPECIFICATIONS UNLESS OTHERWISE NOTED
ALL DIMENSIONS APPLY BEFORE ADDITIVE FINISH
BREAK ALL EDGES AND SHARP CORNERS [ ] MAX.
SURFACE ROUGHNESS ✓ MICRO INCH R.M.S. MAX.
DIAMETERS TO BE CONCENTRIC WITHIN [ ] T.I.R.
FILLET RADIUS [ ] MAX.

MATERIAL —
HEAT TREATMENT —
PROTECTIVE FINISH —

DRAWN BY	W. SOUTAR	DATE 8-15-67
CHECKED BY		DATE 4-6-68
DESIGN APP		DATE 4-8-68
PROJ. ENGR.		DATE

SCHEMATIC-
FEED FORWARD
DISCRIMINATOR

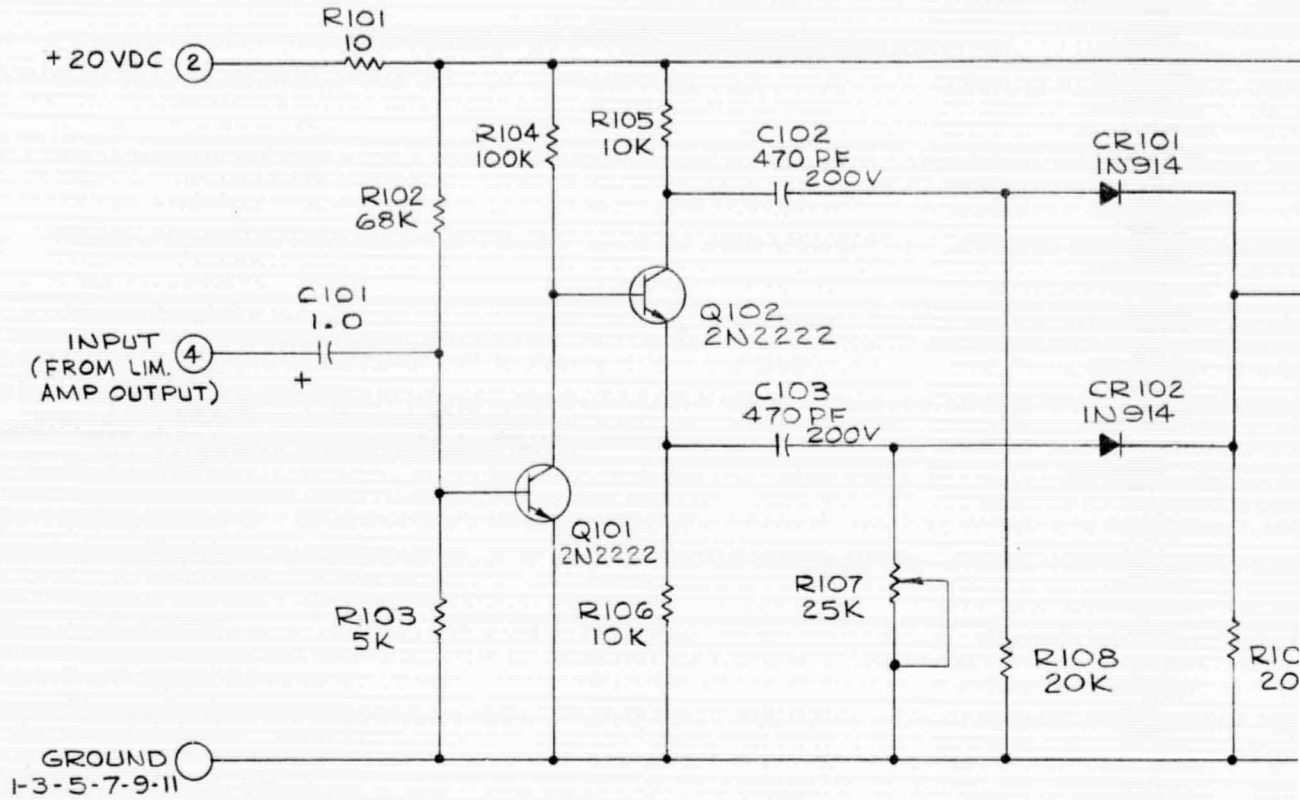
SCALE — DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS —
ANGLES — FRACTIONS —

BORG-WARNER CONTROLS
3300 SO. HALLADAY STREET
SANTA ANA, CALIFORNIA

DWG.		CHG.
C	S-7839	B

C-S-7839 B CHG.

FOLDOUT FRAME 2



2. CAPACITOR VALUES ARE IN MICROFARADS ±10% 35V
1. RESISTOR VALUES ARE IN OHMS, ±5%, 1/4 W.

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT ASSY.	USED ON	PARTS LIST NO.
	APPLICATION	

ITEM	REQ'D	PART NO.
		S/O 76094

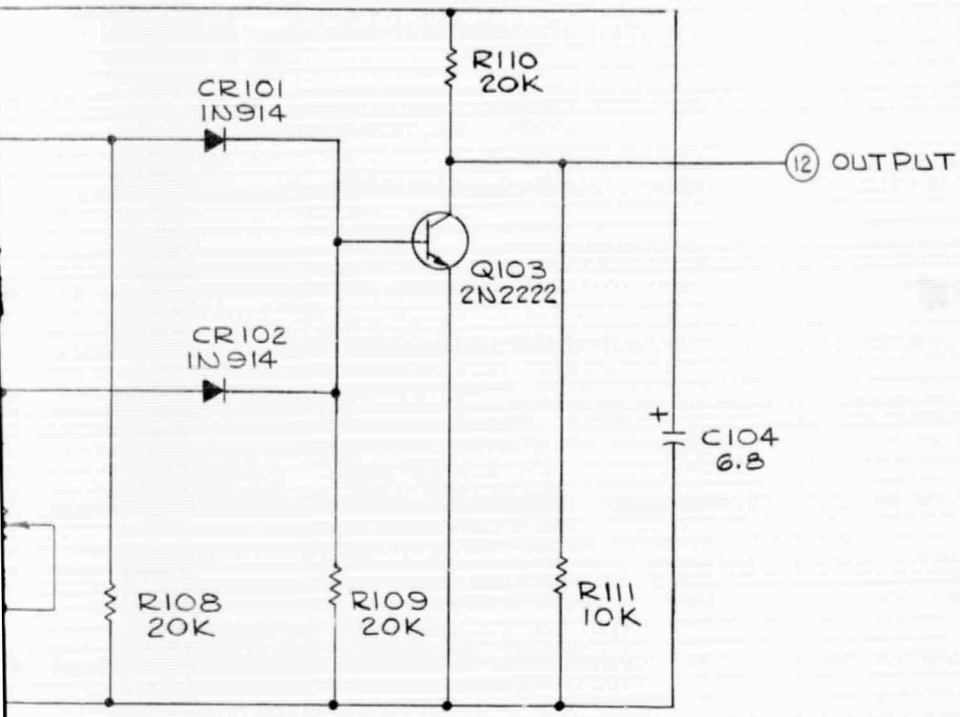
SPECIFICATIONS UNLESS OTHERWISE NOTE

ALL DIMENSIONS APPLY BEFORE ADDITIVE
BREAK ALL EDGES AND SHARP CORNERS
SURFACE ROUGHNESS ✓MICRO INCH R.M
DIAMETERS TO BE CONCENTRIC WITHIN
FILLET RADIUS MAX.

DRAWN BY W. SOUTAR	DATE	10-
CHECKED BY	DATE	4-
DESIGN APP	DATE	4-
PROJ. ENGR.	DATE	

FOLDOUT FRAME 1

REVISIONS					
CHG.	ZONE	DESCRIPTION	E. C. O.	DATE	BY	CHKD



ITEM	REQ'D	PART NO.	DESCRIPTION	MATERIAL	SPEC.	NOTE	SYMBOL
S/O 76094			LIST OF MATERIALS				

SPECIFICATIONS UNLESS OTHERWISE NOTED
ALL DIMENSIONS APPLY BEFORE ADDITIVE FINISH
BREAK ALL EDGES AND SHARP CORNERS [ ] MAX.
SURFACE ROUGHNESS ✓ MICRO INCH R.M.S. MAX.
DIAMETERS TO BE CONCENTRIC WITHIN [ ] T.I.R.
FILLET RADIUS [ ] MAX.

MATERIAL
HEAT TREATMENT
PROTECTIVE FINISH

SCHEMATIC-
PULSE DOUBLER

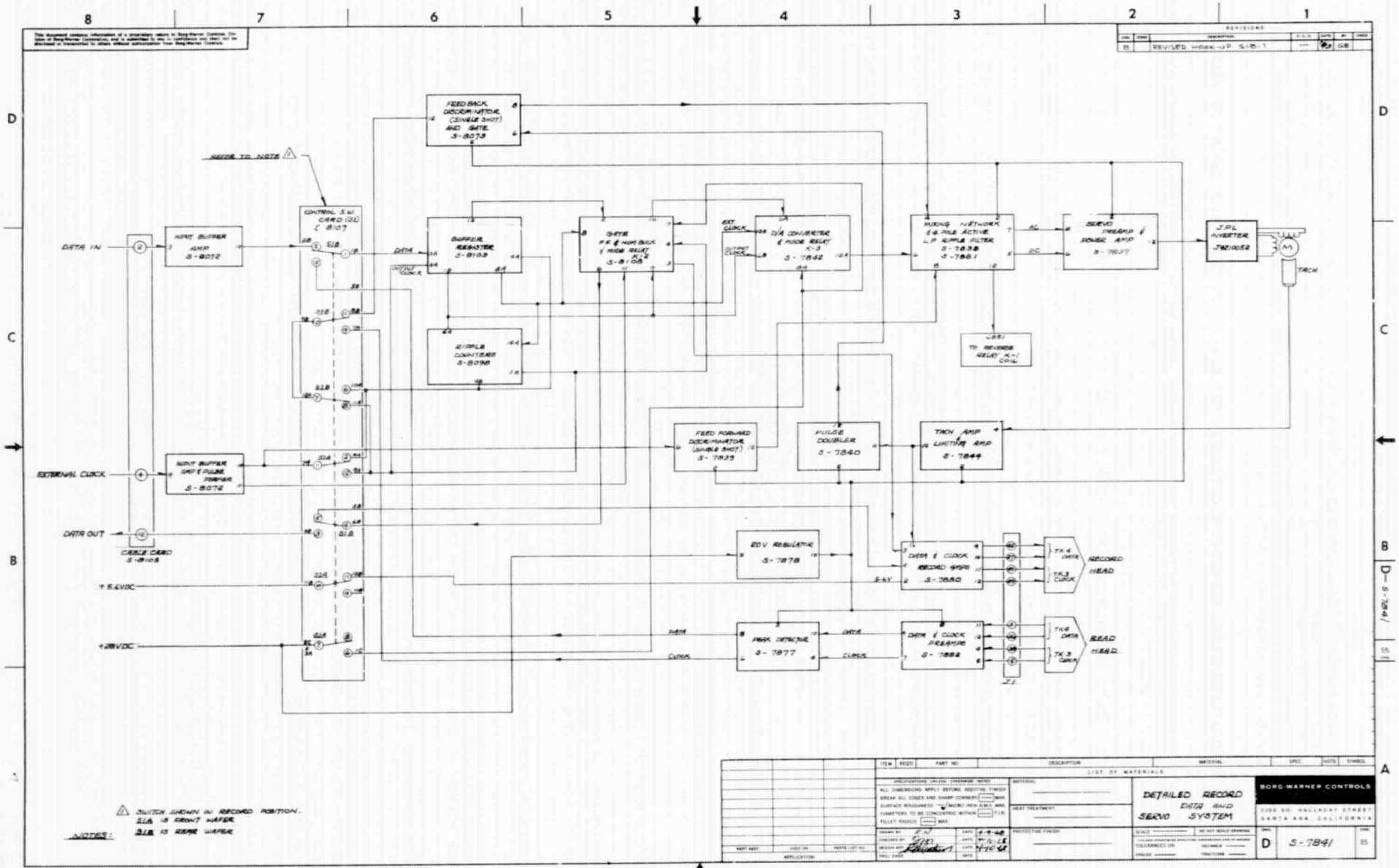
BORG-WARNER CONTROLS
3300 SO. HALLADAY STREET
SANTA ANA, CALIFORNIA

DRAWN BY	W. SOLTAR	DATE 10-14-67
CHECKED BY		DATE 11-8-67
DESIGN APP	[signature]	DATE 1-5-68
PROJ. ENGR.		DATE

SCALE ——— DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS ———
ANGLES ——— FRACTIONS ———

DWG. C S-7840 CHG.

FOLDOUT FRAME 2



REVISIONS

LTR	ZONE	DESCRIPTION	E.C.O.	DATE	BY	CHKD
B		REVISED HOOK-UP S-8-1	—	6-9-68	GB	

LIST OF MATERIALS

ITEM	REQ'D	PART NO.	DESCRIPTION	MATERIAL	SPEC.	NOTE	SYMBOL

ALL DIMENSIONS APPLY BEFORE ADDITIVE FINISH
BREAK ALL EDGES AND SHARP CORNERS .005 MAX.
SURFACE ROUGHNESS 125 MICRO INCH R.M.S. MAX.
DIAMETERS TO BE CONCENTRIC WITHIN .005 T.I.R.
FILLET RADIUS .005 MAX.

Drawn By	E.J.	6-9-68
Checked By		6-10-68
Design Approval		7-10-68
Mfg. Check		

MATERIAL
HEAT TREATMENT
PROTECTIVE FINISH

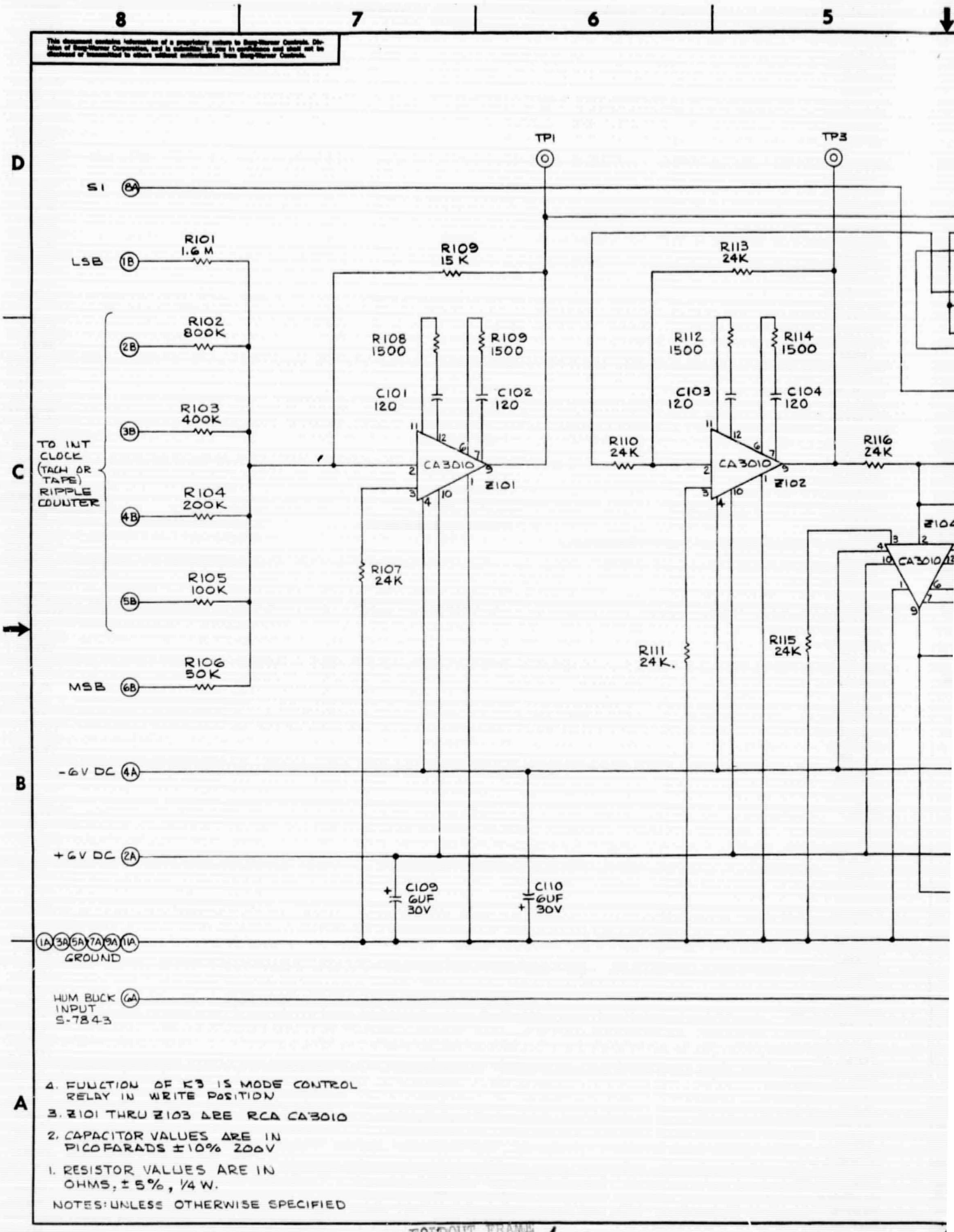
DETAILED RECORD DATA AND SERVO SYSTEM

BORG-WARNER CONTROLS
2100 SO. HALLADAY STREET
SANTA ANA, CALIFORNIA

SCALE — DO NOT SCALE DRAWING
TOLERANCES ON: DECIMALS .xx ANGLES FRACTIONS

DWG. D S-7841 REV. B

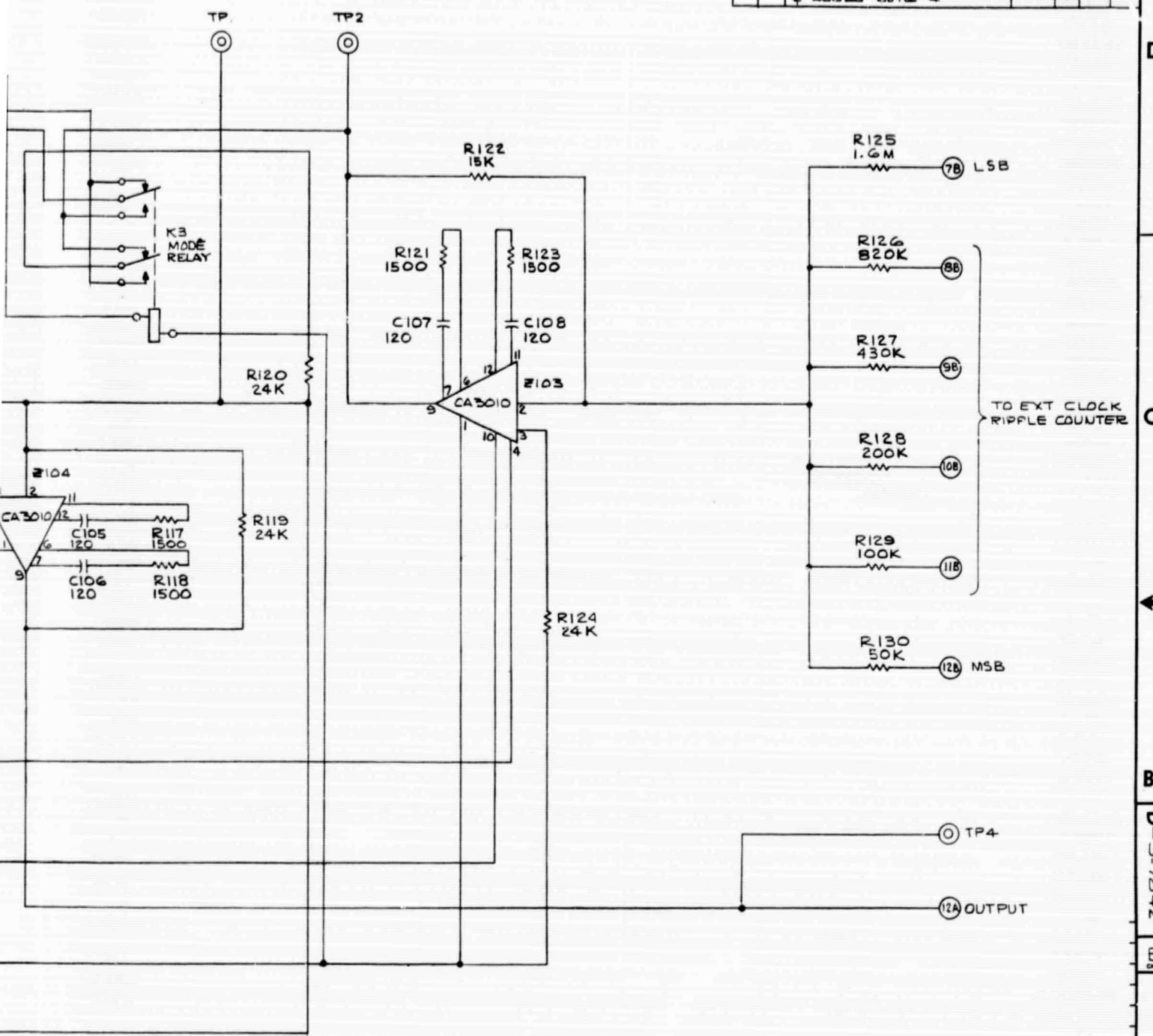
D-S-7841 B



4. FUNCTION OF K3 IS MODE CONTROL RELAY IN WRITE POSITION
3. Z101 THRU Z103 ARE RCA CA3010
2. CAPACITOR VALUES ARE IN PICOFARADS ±10% 200V
1. RESISTOR VALUES ARE IN OHMS, ± 5%, 1/4 W.

NOTES: UNLESS OTHERWISE SPECIFIED

REVISIONS						
CHG.	ZONE	DESCRIPTION	E.C.O.	DATE	BY	CHKD
A		REVISED TEST POINTS; ADDED PIN DESIG, ADDED C109, C110 & K101	—	9/1/65	GE	TG
B		ADDED PIN 6A & REVISED PIN DESIG.; REV RELAY CALLOUT & ADDED NOTE 4	—	9/4/65	GE	



ITEM	REQ'D	PART NO.	DESCRIPTION	MATERIAL	SPEC.	NOTE	SYMBOL

LIST OF MATERIALS

SPECIFICATIONS UNLESS OTHERWISE NOTED:
ALL DIMENSIONS APPLY BEFORE ADDITIVE FINISH
BREAK ALL EDGES AND SHARP CORNERS ☐ MAX.
SURFACE ROUGHNESS ✓ MICRO INCH R.M.S. MAX.
DIAMETERS TO BE CONCENTRIC WITHIN ☐ T.I.R.
FILLET RADIUS ☐ MAX.

MATERIAL
HEAT TREATMENT
PROTECTIVE FINISH

SCHEMATIC
D/A CONVERTER

BORG WARNER-CONTROLS
3300 SO. HALLADAY STREET
SANTA ANA, CALIFORNIA

DRAWN BY	W. SOUTAR	DATE 8-21-67
CHECKED BY		DATE
DESIGN APP.		DATE 4-8-68
PROJ. ENGR.		DATE

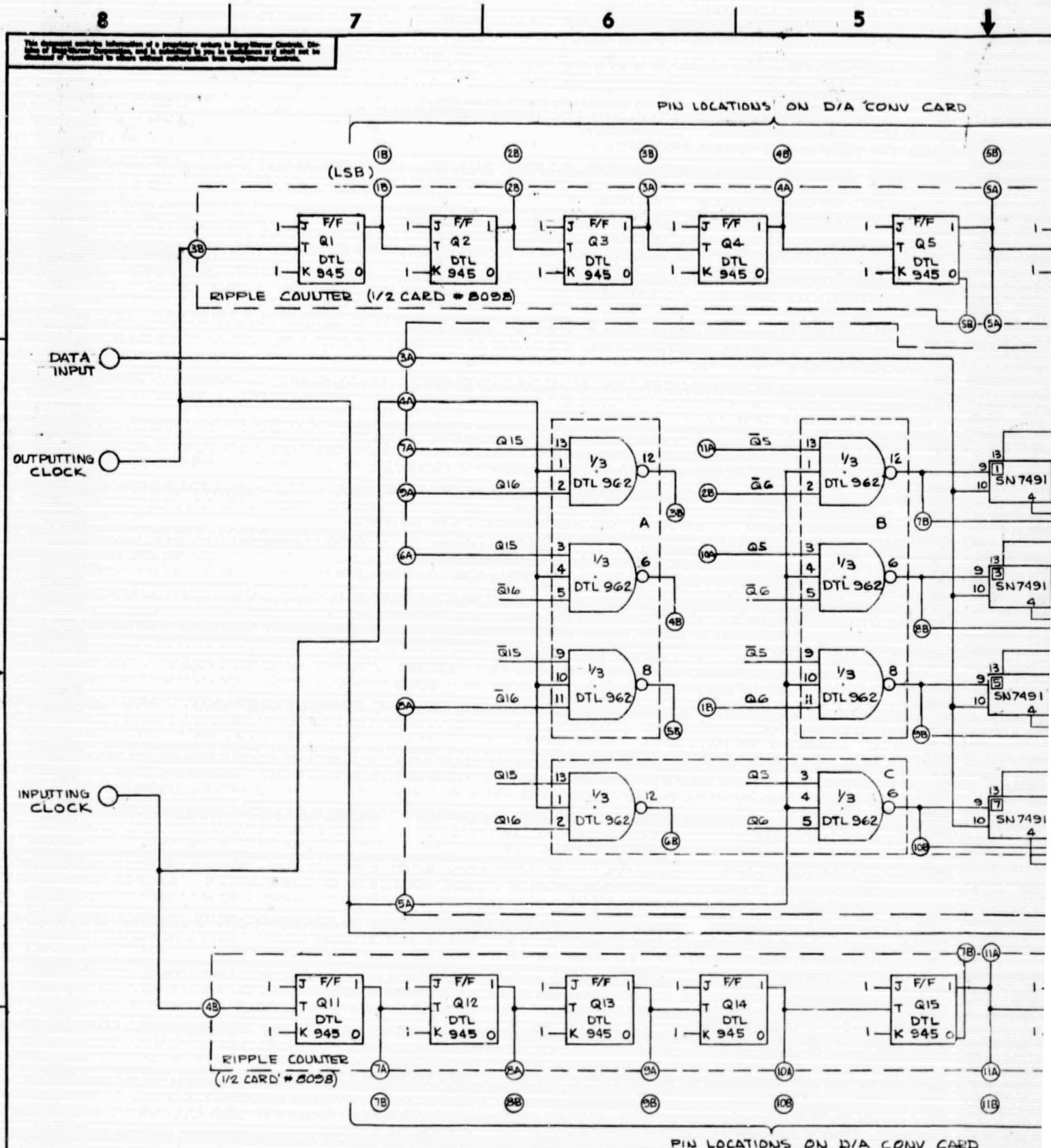
SCALE — DO NOT SCALE DRAWING
TOLERANCES ON DECIMALS —
ANGLES — FRACTIONS —

DWG. D S-7842 CHG. B

NEXT ASSY. | USED ON | PARTS LIST NO.
APPLICATION

FOLDOUT FRAME 2

D-S-7842 B



GFF = GATE FLIP FLOP
RC = RIPPLE COUNTER
BR = BUFFER REGISTER
D/A = DIGITAL TO ANALOG CONVERTER

FOLD OUT FRAME 1

REVISIONS						
CHG.	ZONE	DESCRIPTION	E.C.O.	DATE	BY	CHKD
A		REVISED Q NO'S, ADDED CONNECTIONS TO ALL SW'S REVISED TITLE	—	4/12	GB	

FUNCTION	FROM RC	TO BR
Q5	5A	10A
$\bar{Q}5$	5B	11A
Q6	6A	1B
$\bar{Q}6$	6B	2B
Q15	7B	7A
$\bar{Q}15$	11A	6A
Q16	8B	9A
$\bar{Q}16$	12A	8A

BUFFER REGISTER CARD (#S-8103)

STRAPPING ARRANGEMENT FOR BUFFER REGISTER
(ALSO SHOWN ON INTERCONNECTION DWG #S-8104)

FROM	TO
3B	7B
4B	8B
5B	9B
6B	10B

GATE FLIP FLOP (PART OF S-8108)

DATA OUTPUT

POWER CONNECTIONS TYPICAL

ITEM	REQ'D	PART NO.	DESCRIPTION	MATERIAL	SPEC.	NOTE	SYMBOL
		S/G 76094	LIST OF MATERIALS				

SPECIFICATIONS UNLESS OTHERWISE NOTED
ALL DIMENSIONS APPLY BEFORE ADDITIVE FINISH
BREAK ALL EDGES AND SHARP CORNERS ☐ MAX.
SURFACE ROUGHNESS ✓ MICRO INCH R.M.S. MAX.
DIAMETERS TO BE CONCENTRIC WITHIN ☐ T.I.R.
FILLET RADIUS ☐ MAX.

MATERIAL —
HEAT TREATMENT —
PROTECTIVE FINISH —

SCHEMATIC
DATA BUFFER

BORG-WARNER CONTROLS
3300 SO. HALLADAY STREET
SANTA ANA, CALIFORNIA

DRAWN BY	W. SOUTAR	DATE 8-18-67
CHECKED BY		DATE 4-4-68
DESIGN APP.		DATE 4-5-68
PROJ. ENGR.		DATE

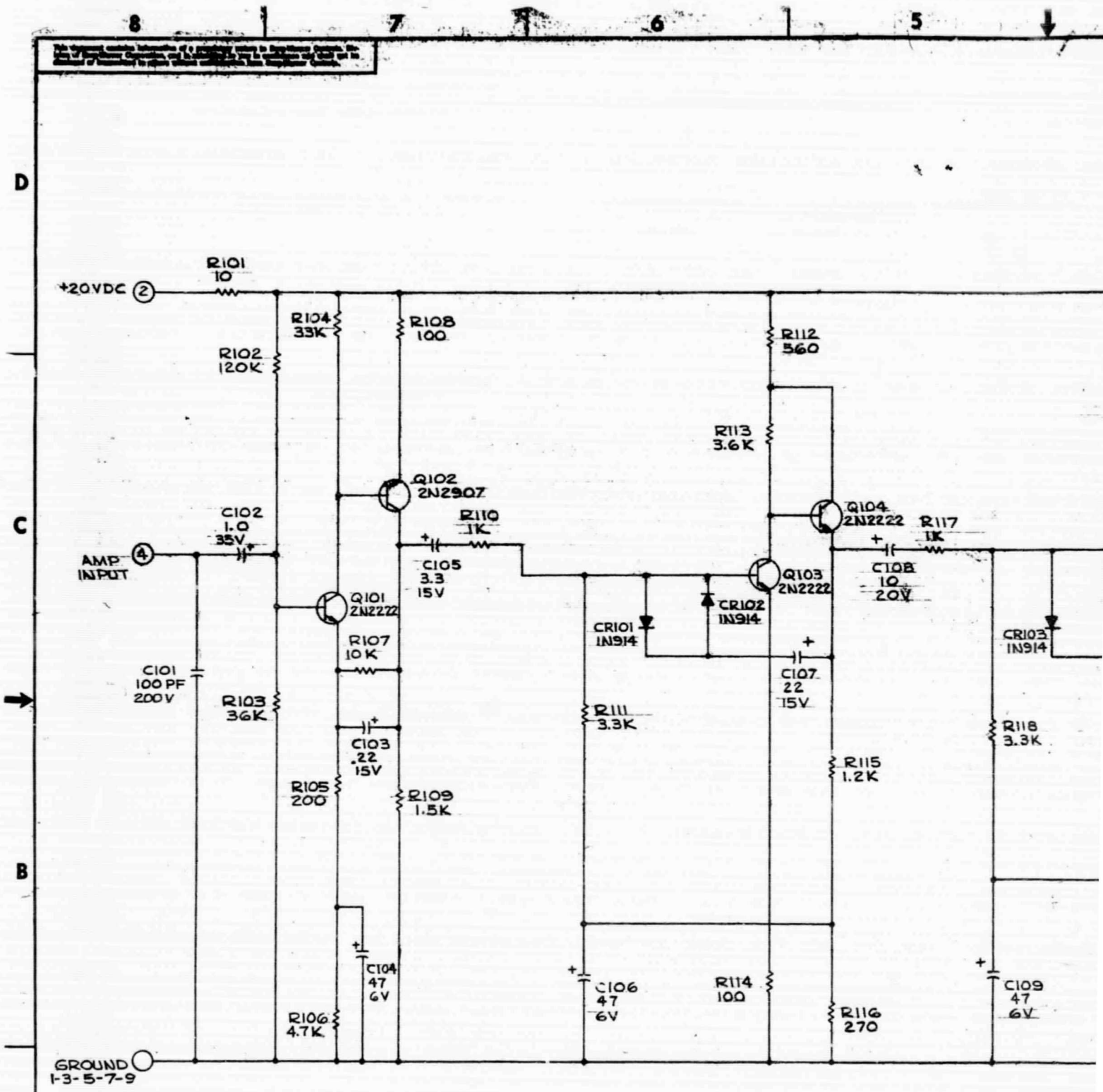
SCALE — DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS —
ANGLES — FRACTIONS —

DWG. D S-7843 CHG. A

NEXT ASSY. | USED ON APPLICATION | PARTS LIST NO.

D-S-7843 A

FOLDOUT FRAME 2

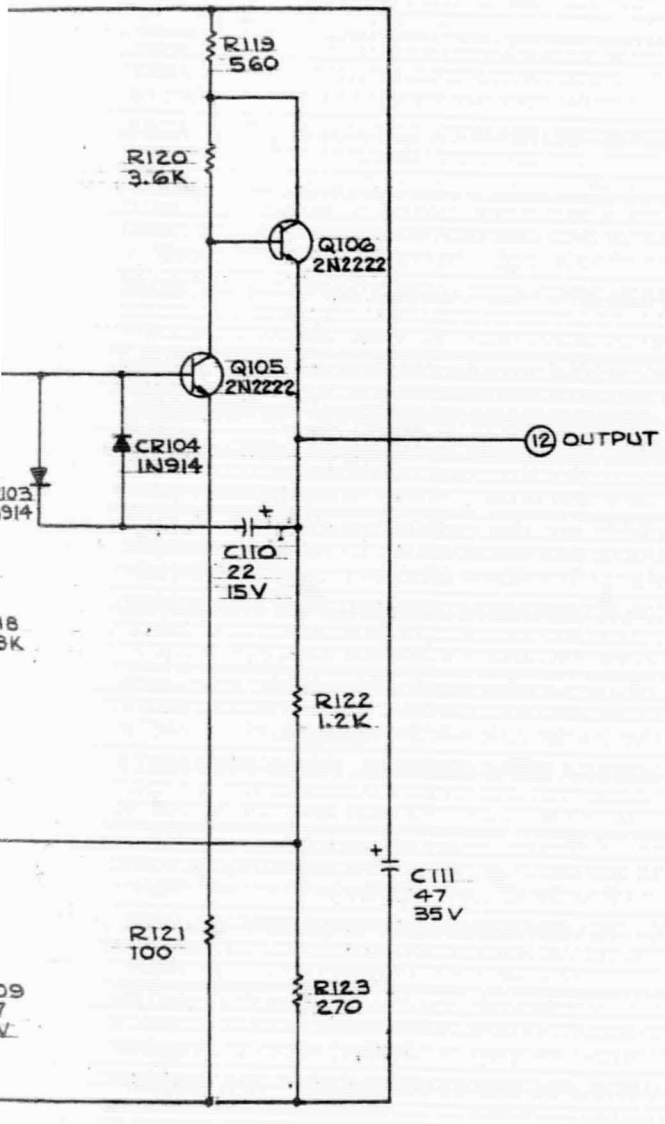


2. CAPACITOR VALUES ARE IN MICROFARADS, ± 10%.
1. RESISTOR VALUES ARE IN OHMS, ± 5%, 1/4 W.

NOTES: UNLESS OTHERWISE SPECIFIED

FOLDOUT FRAME 1

REVISIONS					
CHG	ZONE	DESCRIPTION	E.C.O.	DATE	BY	CHKD
A		DELETED PINS 6 & 8	—	7/6/67	GE	
B		C103 WAS 35V C111 WAS 78@50V	—	7/16/68	GB	12-67



ITEM	REQ'D	PART NO.	DESCRIPTION	MATERIAL	SPEC.	NOTE	SYMBOL
		S/O 76094	LIST OF MATERIALS				

SPECIFICATIONS UNLESS OTHERWISE NOTED
ALL DIMENSIONS APPLY BEFORE ADDITIVE FINISH
BREAK ALL EDGES AND SHARP CORNERS ☐ MAX.
SURFACE ROUGHNESS ✓ MICRO INCH R.M.S. MAX.
DIAMETERS TO BE CONCENTRIC WITHIN ☐ T.I.R.
FILLET RADIUS ☐ MAX.

MATERIAL —
HEAT TREATMENT —
PROTECTIVE FINISH —

SCHEMATIC-
SERVO LIMITING AMPLIFIER

BORG-WARNER CONTROLS
3300 SO. HALLADAY STREET
SANTA ANA, CALIFORNIA

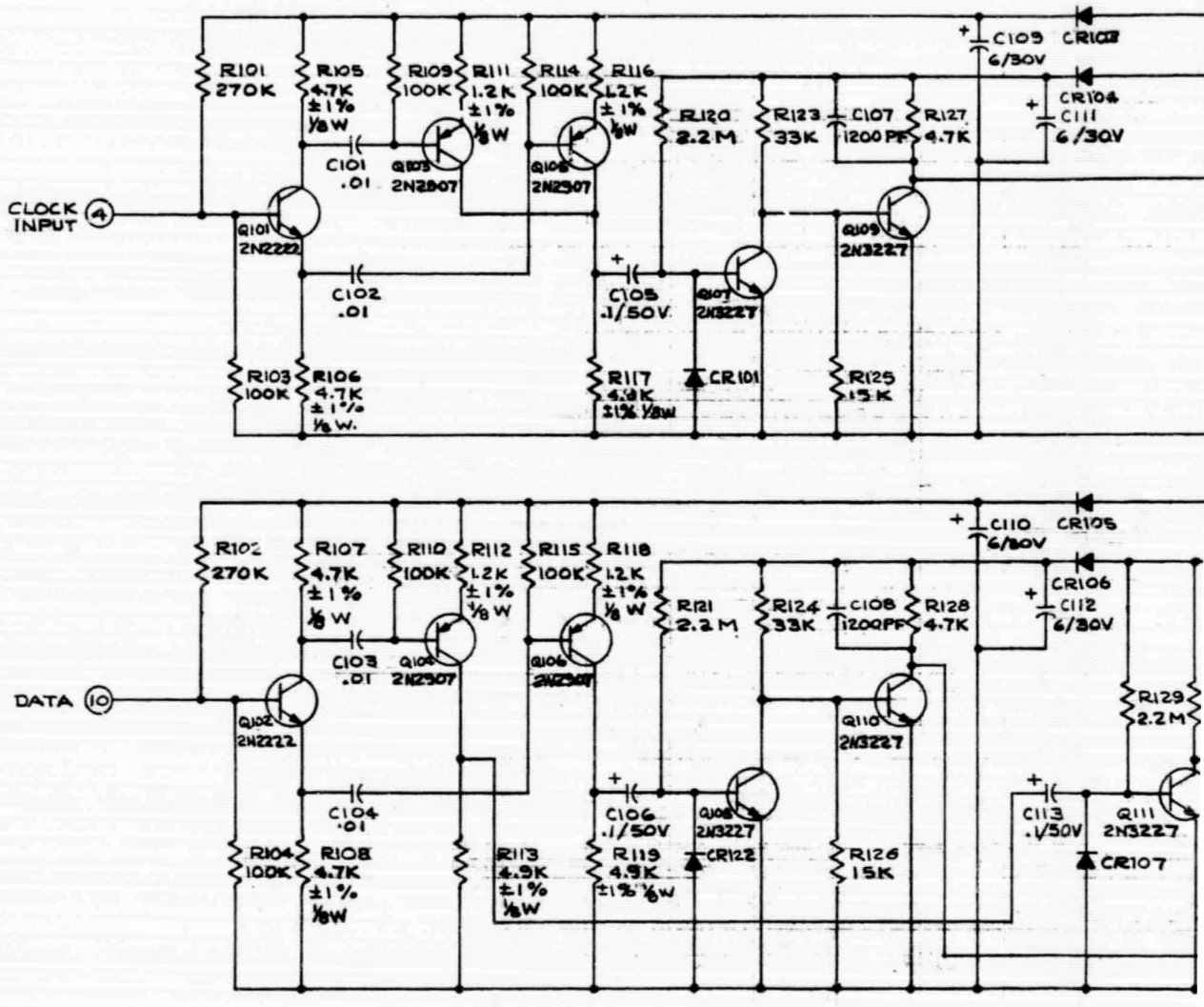
DRAWN BY	W. SOUTAR	DATE 8-15-67
CHECKED BY	Tom	DATE 4-4-68
DESIGN APP.	R. Stanford	DATE 4-8-68
PROJ. ENGR.		DATE

SCALE — DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS —
ANGLES — FRACTIONS —

DWG. D S-7844 CHG. B

NEXT ASSY. | USED ON | PARTS LIST NO.
APPLICATION

FOLDOUT FRAME 2



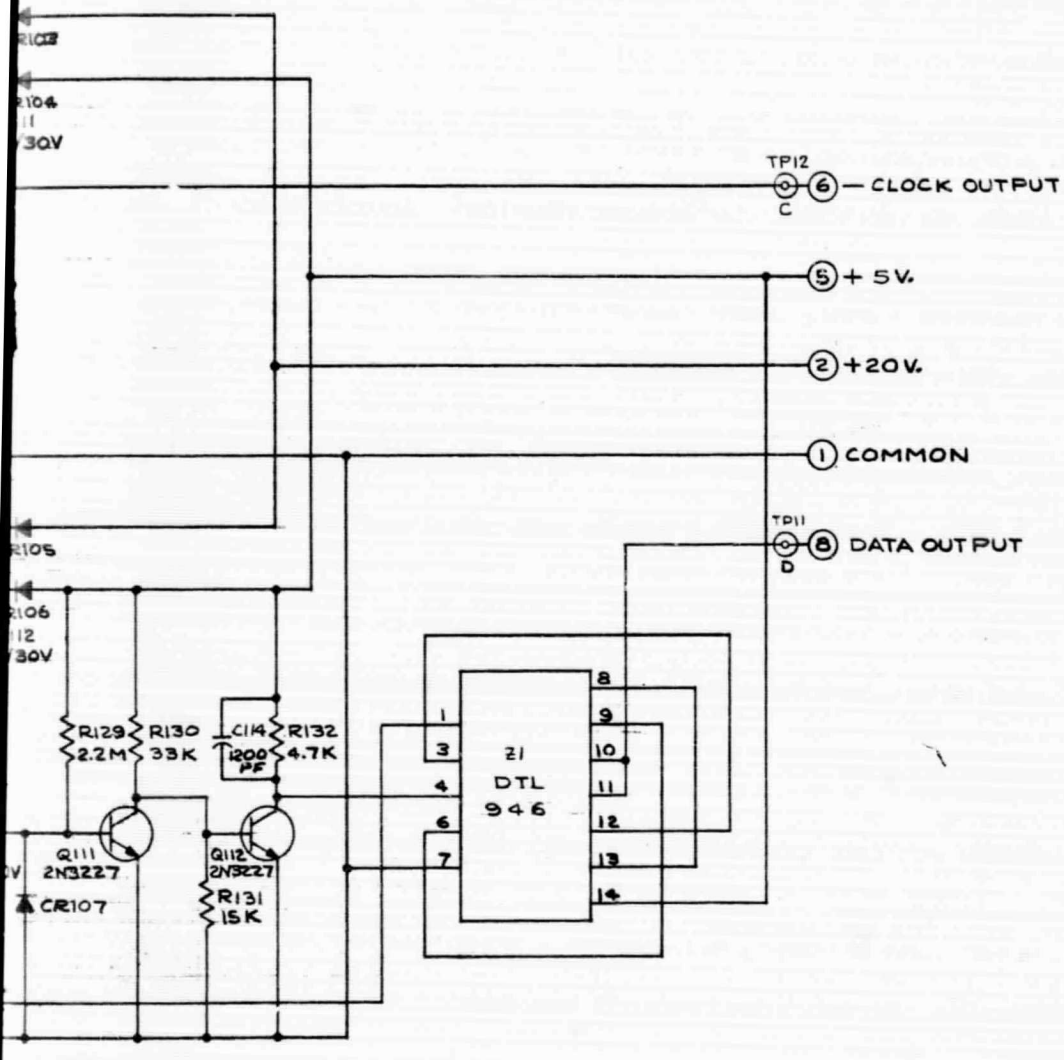
3. DIODES ARE IN914.

2. CAPACITOR VALUES ARE IN MICROFARADS, ±10%, 200V.

1. RESISTOR VALUES ARE IN OHMS, ±5%, 1/4W.

NOTES: UNLESS OTHERWISE SPECIFIED

REVISIONS						
CHG.	ZONE	DESCRIPTION	E.C.O.	DATE	BY	CHKD
B		REVISED & REDRAWN	—	11/6/	PF	



ITEM	REQ'D	PART NO.	DESCRIPTION	MATERIAL	SPEC.	NOTE	SYMBOL

LIST OF MATERIALS

SPECIFICATIONS UNLESS OTHERWISE NOTED
ALL DIMENSIONS APPLY BEFORE ADDITIVE FINISH
BREAK ALL EDGES AND SHARP CORNERS — MAX.
SURFACE ROUGHNESS ✓ MICRO INCH R.M.S. MAX.
DIAMETERS TO BE CONCENTRIC WITHIN — T.I.R.
FILLET RADIUS — M.V.

MATERIAL
HEAT TREATMENT
PROTECTIVE FINISH

DRAWN BY Phil Trowbridge	DATE	4-5-68
CHECKED BY [illegible]	DATE	4-8-68
DESIGN APP.	DATE	
PROJ. ENGR.	DATE	

SCHEMATIC
PEAK
DETECTOR

BORG WARNER CONTROLS
3300 SO. HALLADAY STREET
SANTA ANA, CALIFORNIA

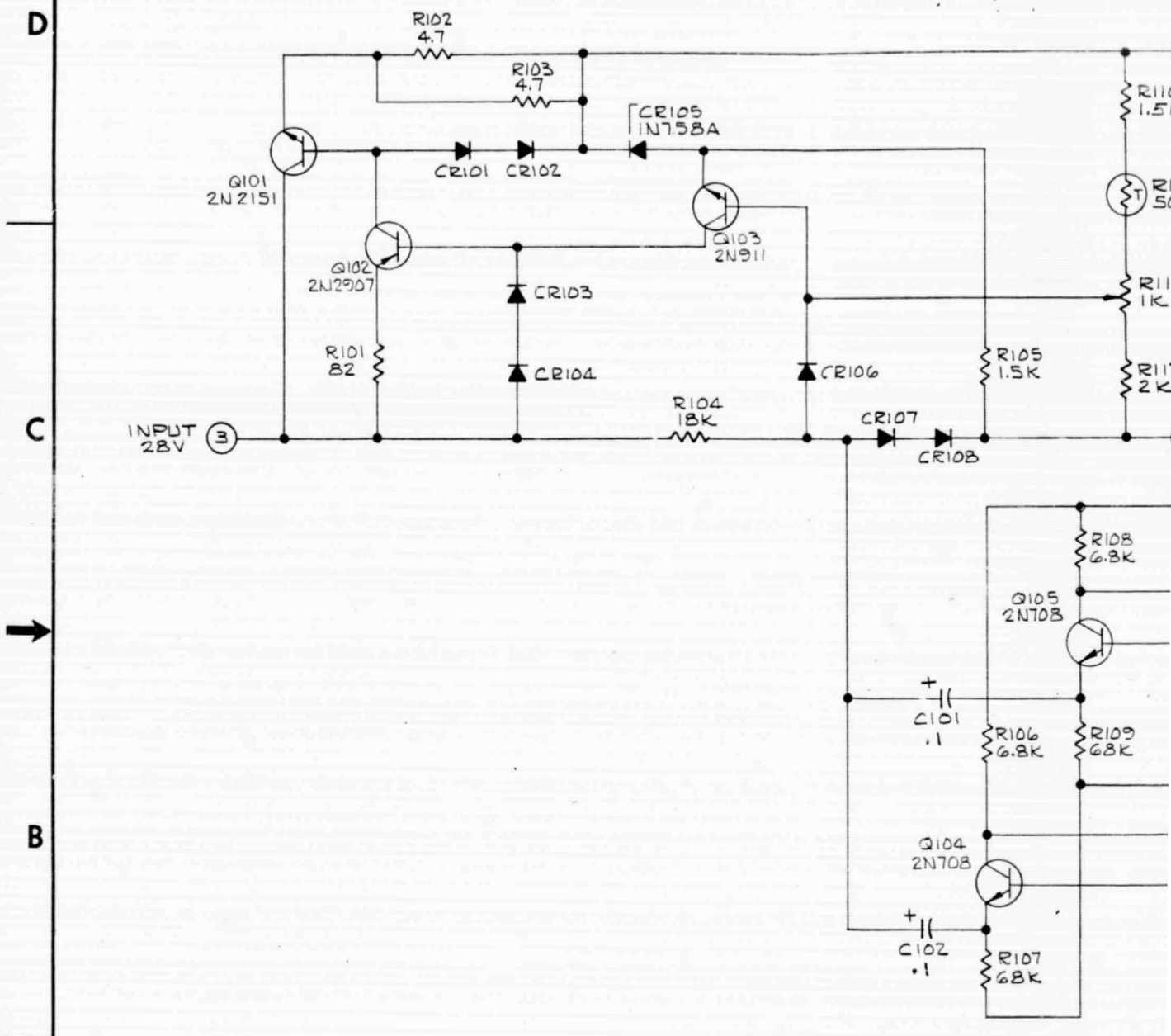
SCALE — DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS
ANGLES FRACTIONS

DWG. D S-7877 CHG. B

NEXT ASSY. | USED ON | PARTS LIST NO.
APPLICATION

D-S-7877-01

FOLDOUT FRAME 2



4. V101 & V102 ARE HOFFMAN SOLAR CELL 52C
3. CAPACITOR VALUES ARE IN MICROFARADS ±10% 35V
2. DIODES ARE IN485B
1. RESISTOR VALUES ARE IN OHMS ± 5% 1/4 W

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT ASSY.	USED ON	PARTS LIST NO.
	APPLICATION	

ITEM	REQ'D	PART NO.
		510 76094

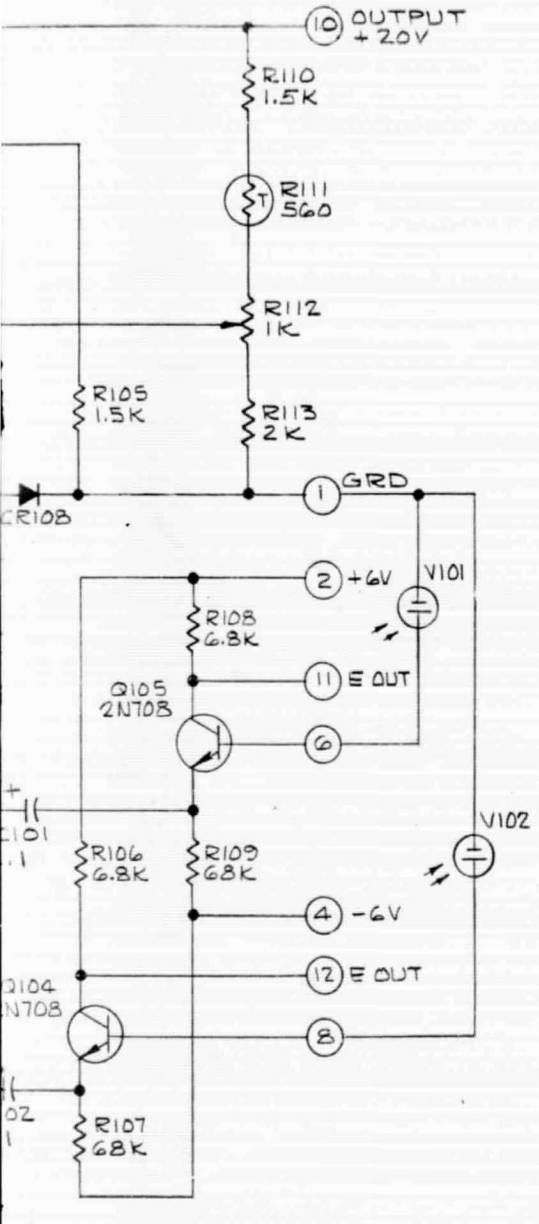
SPECIFICATIONS UNLESS OTHERWISE NOTED

ALL DIMENSIONS APPLY BEFORE ADDITIVE FINISH
BREAK ALL EDGES AND SHARP CORNERS — MAX
SURFACE ROUGHNESS ✓ MICRO INCH R.M.S. MAX
DIAMETERS TO BE CONCENTRIC WITHIN — T.I.R.
FILLET RADIUS — MAX.

DRAWN BY G. EVANS	DATE	3-18-6
CHECKED BY J.E. HUMES	DATE	3-14-6
DESIGN APP. R. Hightower	DATE	4-8-6
PROJ. ENGR.	DATE	

FOLDOUT FRAME

REVISIONS						
CHG.	ZONE	DESCRIPTION	E. C. O.	DATE	BY	CHKD
A		ADDED NOTES 3 & 4; REVISED SYMBOL OF SOLAR CELL	—	3/12/68	GE	V. E. H.



REQ'D	PART NO.	DESCRIPTION	MATERIAL	SPEC.	NOTE	SYMBOL
	76084	LIST OF MATERIALS				

SPECIFICATIONS UNLESS OTHERWISE NOTED
DIMENSIONS APPLY BEFORE ADDITIVE FINISH
BREAK ALL EDGES AND SHARP CORNERS — MAX.
SURFACE ROUGHNESS ✓ MICRO INCH R.M.S. MAX.
HOLES TO BE CONCENTRIC WITHIN — T.I.R.
FILLET RADIUS — MAX.

MATERIAL —

HEAT TREATMENT —

PROTECTIVE FINISH —

SCHEMATIC
20 V REG. & EOT
& BOT SENSORS

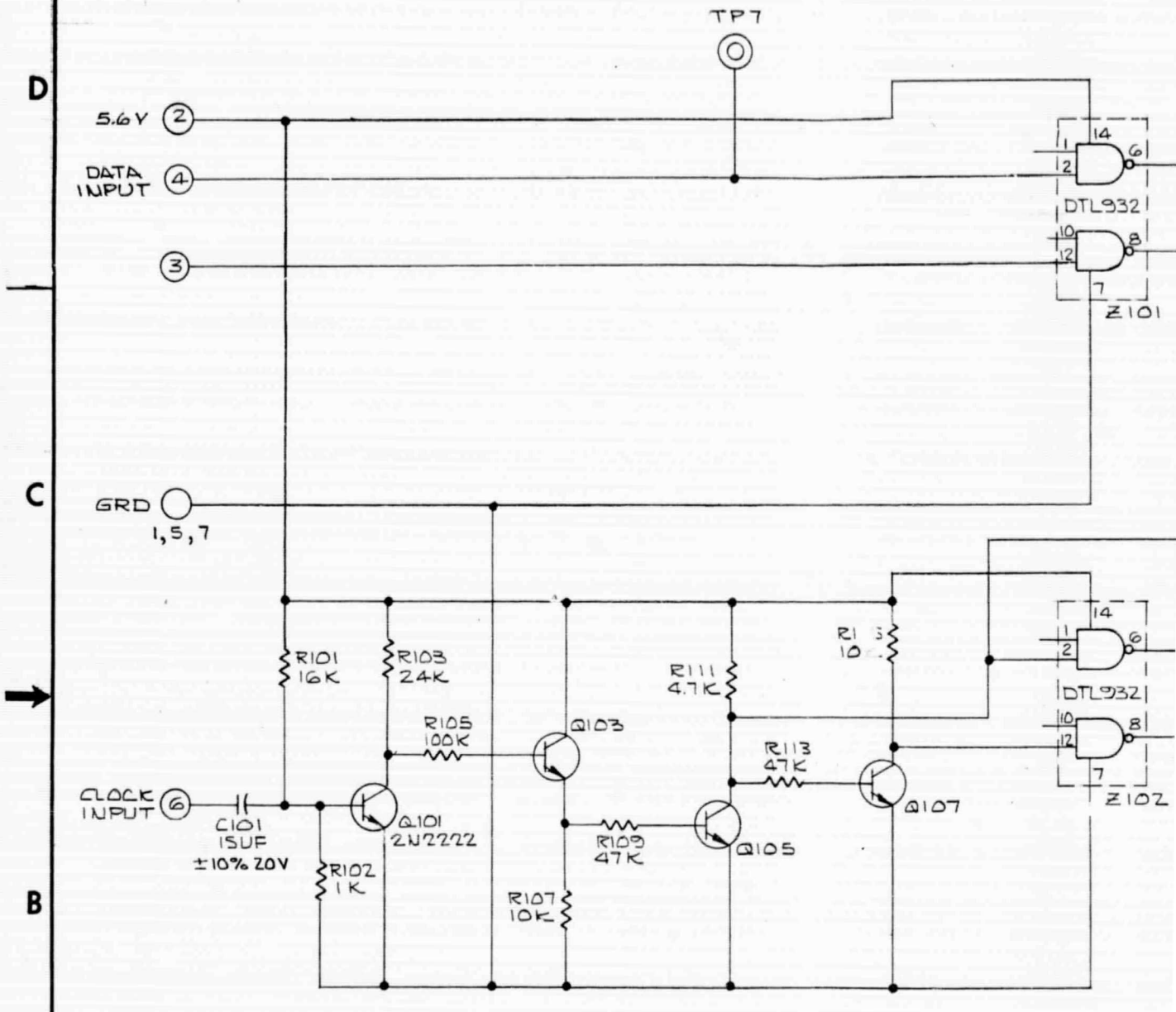
BORG-WARNER CONTROLS
3300 SO. HALLADAY STREET
SANTA ANA, CALIFORNIA

DRAWN BY G. EVANS	DATE	5-18-67
CHECKED BY J. E. HUMES	DATE	3-14-68
APPROVED BY R. Kilpatrick	DATE	4-8-68
ENGR.	DATE	

SCALE — DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS —
ANGLES — FRACTIONS —

DWG. C S-7878 CHG. A

FOLDOUT FRAME 2



2. TRANSISTORS ARE 2N3227

1. RESISTOR VALUES ARE IN OHMS ±5% 1/4 W

NOTES: UNLESS OTHERWISE SPECIFIED

ITEM	REQ'D	PART NO.
		510 76029

SPECIFICATIONS UNLESS OTHERWISE NOTED

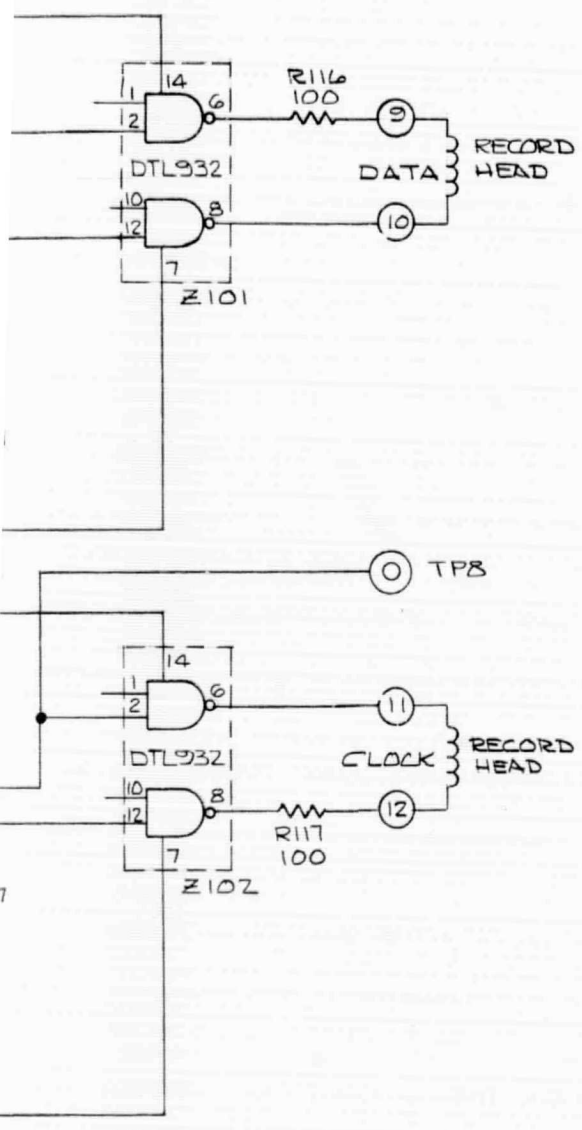
ALL DIMENSIONS APPLY BEFORE ADDITIVE FINISH
BREAK ALL EDGES AND SHARP CORNERS ____ MAX.
SURFACE ROUGHNESS √ MICRO INCH R.M.S. MAX.
DIAMETERS TO BE CONCENTRIC WITHIN ____ T.I.R.
FILLET RADIUS ____ MAX.

DRAWN BY G. EVANS	DATE	9-18-6
CHECKED BY	DATE	4-4-68
DESIGN APP	DATE	4-4-68
PROJ. ENGR.	DATE	

NEXT ASSY.	USED ON	PARTS LIST NO.
	APPLICATION	

FOLDOUT FRAME 1

REVISIONS						
CHG.	ZONE	DESCRIPTION	E.C.O.	DATE	BY	CHKD
A		DELETED R104, R106, R108, R110, R112, R114, Q102, Q104, Q106; ADD PIN 3 & TP7 & TP8	—	9/9/68	GE	



D	PART NO.	DESCRIPTION	MATERIAL	SPEC.	NOTE	SYMBOL
	76029					

LIST OF MATERIALS

CATIONS UNLESS OTHERWISE NOTED
IONS APPLY BEFORE ADDITIVE FINISH
EDGES AND SHARP CORNERS — MAX.
UGHNESS ✓ MICRO INCH R.M.S. MAX.
TO BE CONCENTRIC WITHIN — T.I.R.
US — MAX.

MATERIAL —

HEAT TREATMENT —

PROTECTIVE FINISH —

SCHEMATIC
DATA & CLOCK
RECORD AMPL

BORG-WARNER CONTROLS
3300 SO. HALLADAY STREET
SANTA ANA, CALIFORNIA

EVANS	DATE	9-18-67
	DATE	4-8-68
	DATE	4-8-68
	DATE	

SCALE — DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS —
ANGLES — FRACTIONS —

DWG. C | S-7880 | CHG. A

FOLDOUT FRAME 2

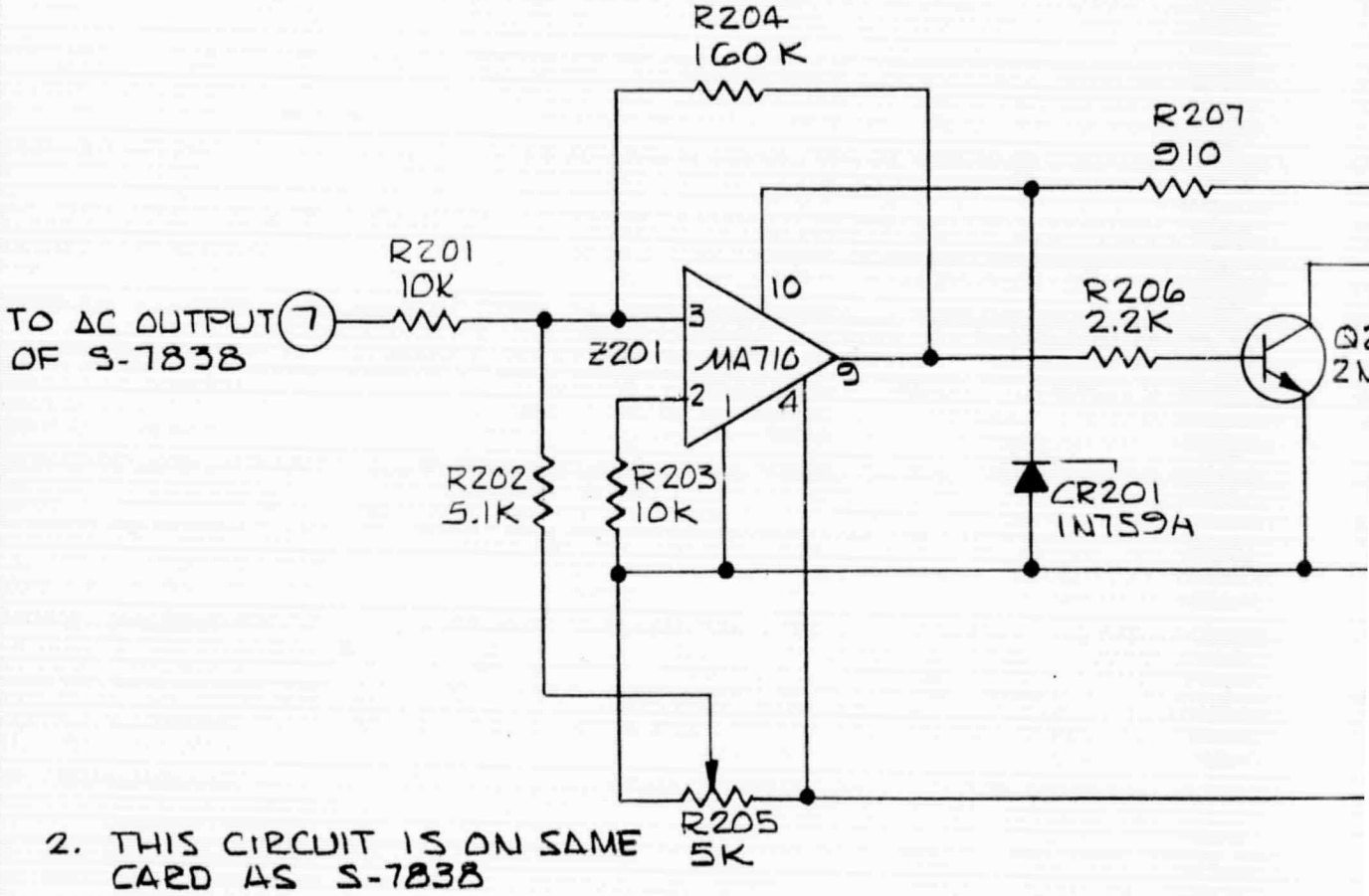
5 4

D

C

B

A



2. THIS CIRCUIT IS ON SAME CARD AS S-7838

1. RESISTOR VALUES ARE IN OHMS ± 5% 1/4W

NOTES: UNLESS OTHERWISE SPECIFIED

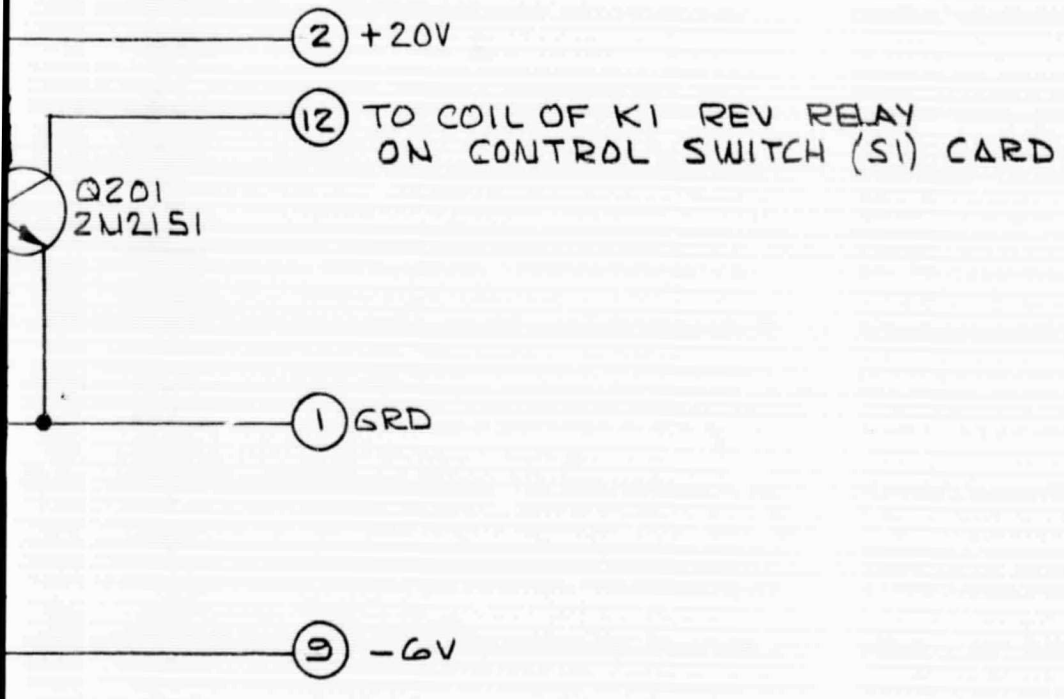
			ITEM	REQ'D	PART NO.	
					S10 76094	
			SPECIFICATIONS UNLESS OTHERWISE NOTED			MATERIAL
			ALL DIMENSIONS APPLY BEFORE ADDITIVE FINISH			
			BREAK ALL EDGES AND SHARP CORNERS ——— MAX.			
			SURFACE ROUGHNESS —√ MICRO INCH R.M.S. MAX.			HEAT TREATM
			DIAMETERS TO BE CONCENTRIC WITHIN ——— T.I.R.			
			FILLET RADIUS ——— MAX.			
			DRAWN BY G. EVANS	DATE	9-18-67	PROTECTIVE
			CHECKED BY	DATE	4-8-68	
NEXT ASSY.	USED ON	PARTS LIST NO.	DESIGN APP.	DATE	4-8-68	
APPLICATION			PROJ. ENGR.	DATE		

FOLDOUT FRAME 1

3	B- S-7881	A CHG.	2	1

REVISIONS

CHG.	ZONE	DESCRIPTION	E. C. O.	DATE	BY	CHKD
A		ADDED VALUE OF R204; CR201 WAS IN750; ADDED NOTE 2	——	3/14/68	GE	V. E. H.

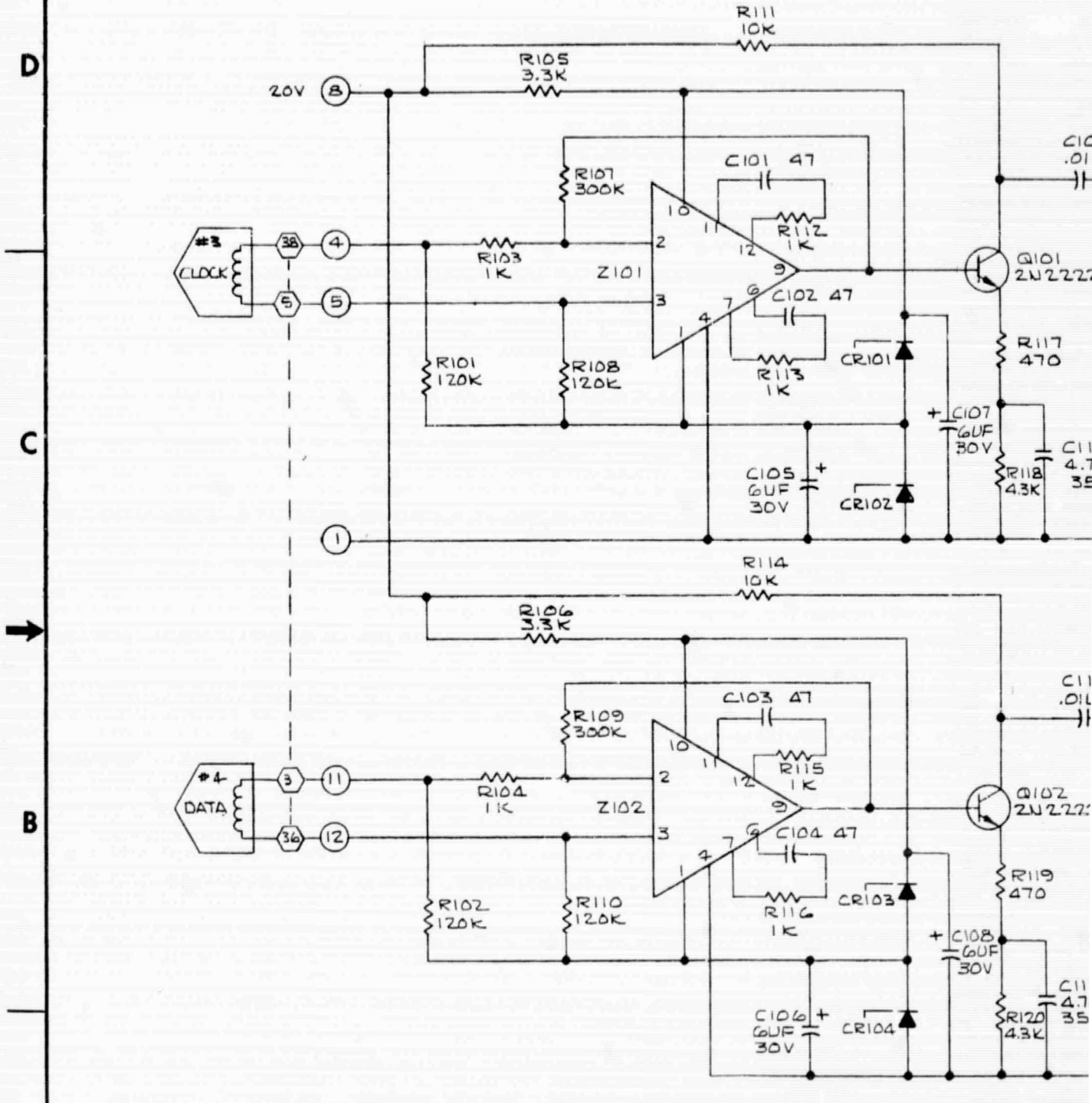


DESCRIPTION	MATERIAL	SPEC.	NOTE	SYMBOL

LIST OF MATERIALS

ERIAL ——	SCHEMATIC REVERSE RELAY DRIVER	BORG-WARNER CONTROLS
T TREATMENT ——		3300 SO. HALLADAY STREET SANTA ANA, CALIFORNIA
TECTIVE FINISH ——	SCALE —— DO NOT SCALE DRAWING	DWG. B S-7881 CHG. A
	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS —— ANGLES —— FRACTIONS ——	

POUDOUT FRAME 2



5. ⬡ REFER TO J1 ON TAPE TRANSPORT
4. Z101 & Z102 ARE RCA CA3010
3. DIODES ARE 1N751
2. CAPACITOR VALUES ARE IN PICOFARADS ±10% 200V
1. RESISTOR VALUES ARE IN OHMS ±5% 1/4 W

NOTES: UNLESS OTHERWISE SPECIFIED

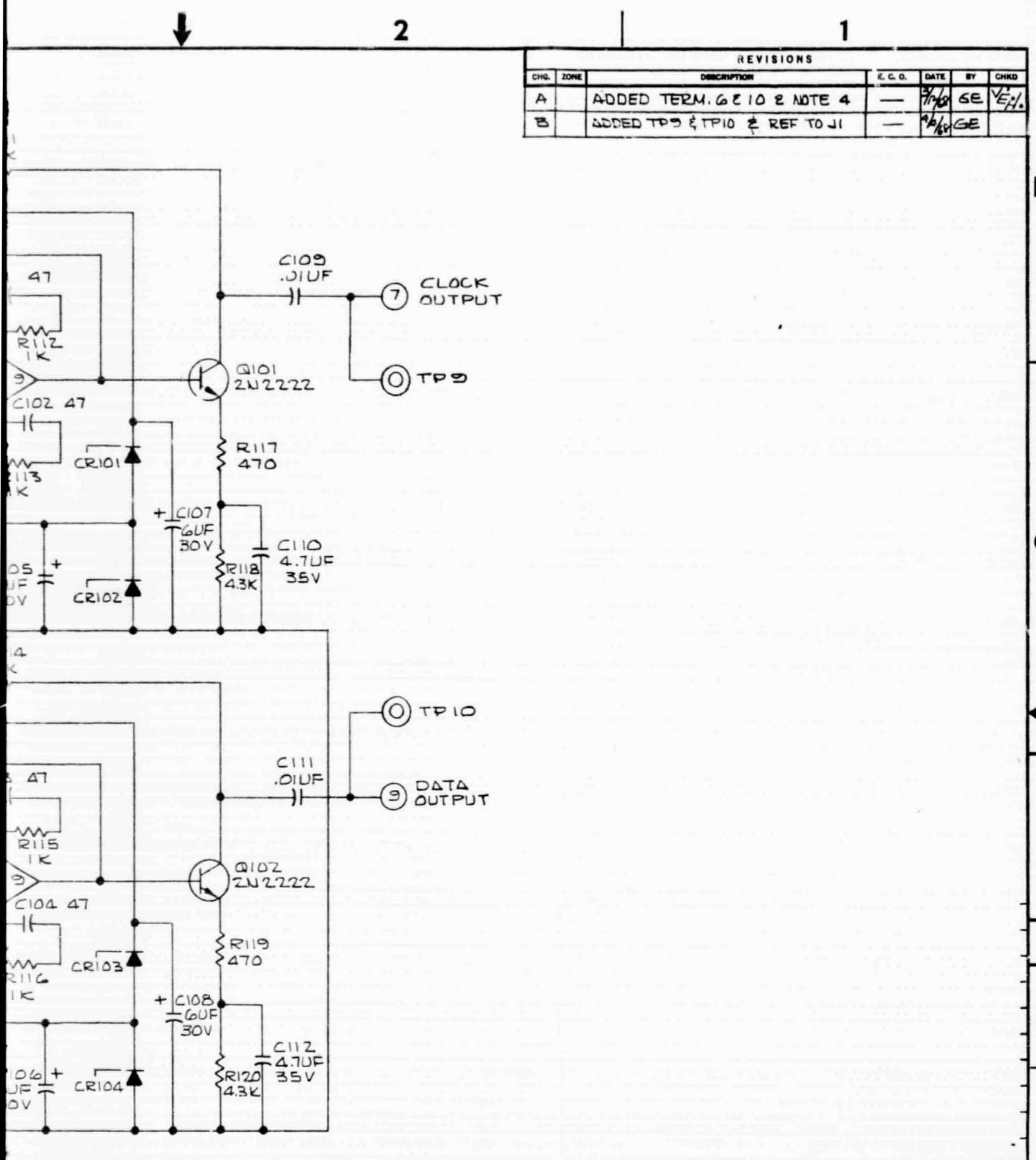
NEXT ASSY.	USED ON	PARTS LIST NO.
APPLICATION		

ITEM	REQ'D	PART NO.
		510 76054

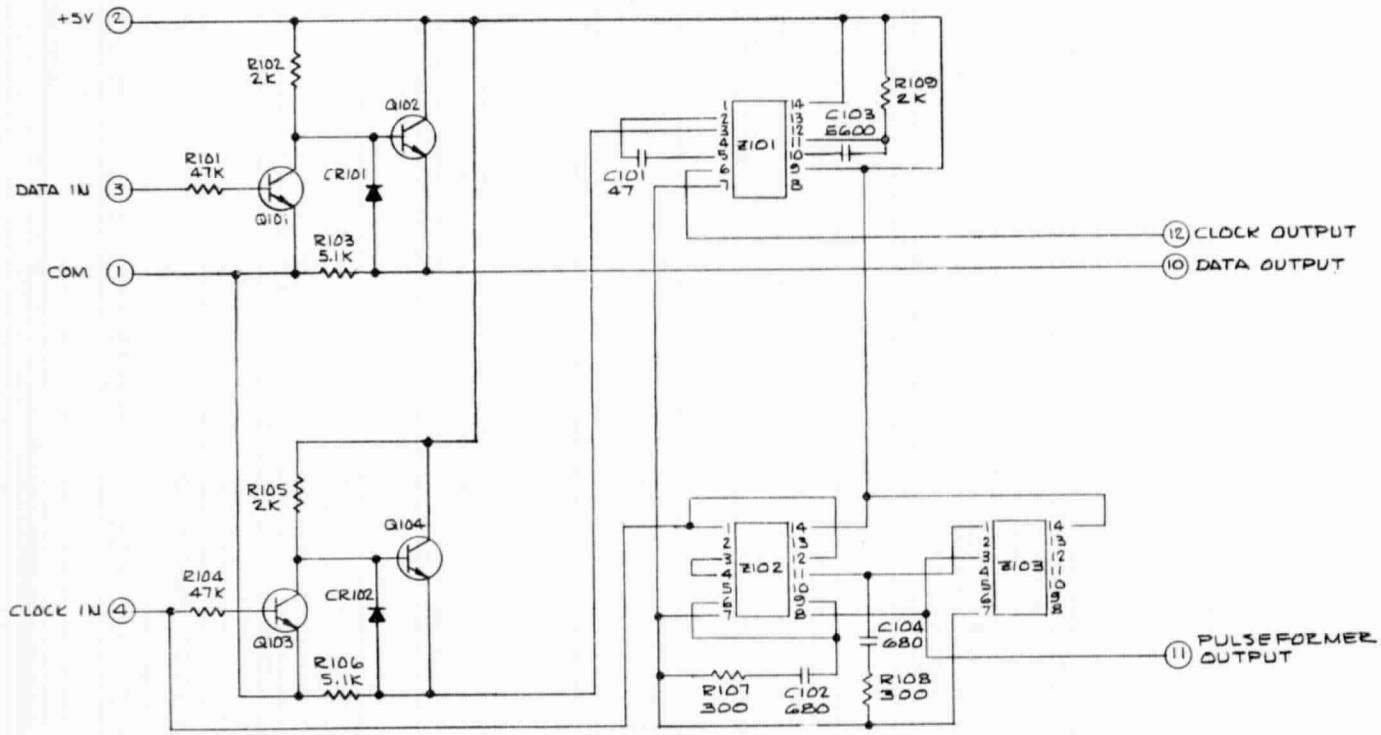
SPECIFICATIONS UNLESS OTHERWISE NOTED

ALL DIMENSIONS APPLY BEFORE ADDITIVE FINISH
BREAK ALL EDGES AND SHARP CORNERS — MAX.
SURFACE ROUGHNESS √ MICRO INCH R.M.S. MAX.
DIAMETERS TO BE CONCENTRIC WITHIN — T.I.R.
FILLET RADIUS — MAX.

DRAWN BY G. EVANS	DATE	9-18-67
CHECKED BY	DATE	
DESIGN APP.	DATE	9-8-67
PROJ. ENGR.	DATE	


2
1
REVISIONS
CHG. | ZONE | DESCRIPTION | E. C. O. | DATE | BY | CHKD
A | | ADDED TERM. 6 & 10 & NOTE 4 | — | 3/7/68 | GE | VE.H.
B | | ADDED TP9 & TP10 & REF TO J1 | — | 4/26/68 | GE |
D
C
B
A
C109 .01UF
7 CLOCK OUTPUT
9 TP9
Q101 2N2222
R112 1K
C102 47
R113 1K
CR101
R117 470
C107 6UF 30V
C110 4.7UF 35V
R118 4.3K
CR102
47
C105 .05UF 30V
10 TP10
C111 .01UF
3 DATA OUTPUT
Q102 2N2222
R115 1K
C104 47
R116 1K
CR103
R119 470
C108 6UF 30V
C112 4.7UF 35V
R120 4.3K
CR104
C106 .05UF 30V
C
S-7882
B
CHG.
B
A
ITEM | REQ'D | PART NO. | DESCRIPTION | MATERIAL | SPEC. | NOTE | SYMBOL
510 76054
LIST OF MATERIALS
SPECIFICATIONS UNLESS OTHERWISE NOTED
ALL DIMENSIONS APPLY BEFORE ADDITIVE FINISH
BREAK ALL EDGES AND SHARP CORNERS — MAX.
SURFACE ROUGHNESS √ MICRO INCH R.M.S. MAX.
DIAMETERS TO BE CONCENTRIC WITHIN — T.I.R.
FILLET RADIUS — MAX.
MATERIAL
HEAT TREATMENT
PROTECTIVE FINISH
SCHEMATIC
CLOCK & DATA
PREAMPLIFIER
BORG-WARNER CONTROLS
3300 SO. HALLADAY STREET
SANTA ANA, CALIFORNIA
DRAWN BY G. EVANS DATE 9-18-67
CHECKED BY DATE
DESIGN APP. DATE 9-8-67
PROJ. ENGR. DATE
SCALE — DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS —
ANGLES — FRACTIONS —
DWG. C
S-7882
CHG. B
FOLDOUT FRAME 2

REVISIONS						
CHG.	ZONE	DESCRIPTION	E.C.O.	DATE	BY	CHKD
D		ADDED Z101 102 & 103 ADDED R107 108 & 109 ADDED C101 C102 103 & 104	—	4/9/68	GE	
B		ADDED CONJECTION BETWEEN R102 & R105	—	4/18/68	GE	



5. Z101, 102 & 103 ARE DTL 946
4. DIODES ARE IN914
3. TRANSISTORS ARE 2N2222
2. CAPACITOR VALUES ARE IN PICOFARADS ±10% 200V
1. RESISTOR VALUES ARE IN OHMS ±5% 1/4W

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT ASSY.	USED ON	PARTS LIST NO.
APPLICATION		

ITEM	REQ'D	PART NO.	DESCRIPTION	MATERIAL	SPEC.	NOTE	SYMBOL

LIST OF MATERIALS

SPECIFICATIONS UNLESS OTHERWISE NOTED
ALL DIMENSIONS APPLY BEFORE ADDITIVE FINISH
BREAK ALL EDGES AND SHARP CORNERS ☐ MAX.
SURFACE ROUGHNESS √ MICRO INCH R.M.S. MAX.
DIAMETERS TO BE CONCENTRIC WITHIN ☐ T.I.R.
FILLET RADIUS ☐ MAX.

DRAWN BY	G. EVANS	DATE 4-5-68
CHECKED BY	[illegible]	DATE 4-8-68
DESIGN APP.	[illegible]	DATE 4-9-68
PROJ. ENGR.		DATE

MATERIAL —
HEAT TREATMENT —
PROTECTIVE FINISH —

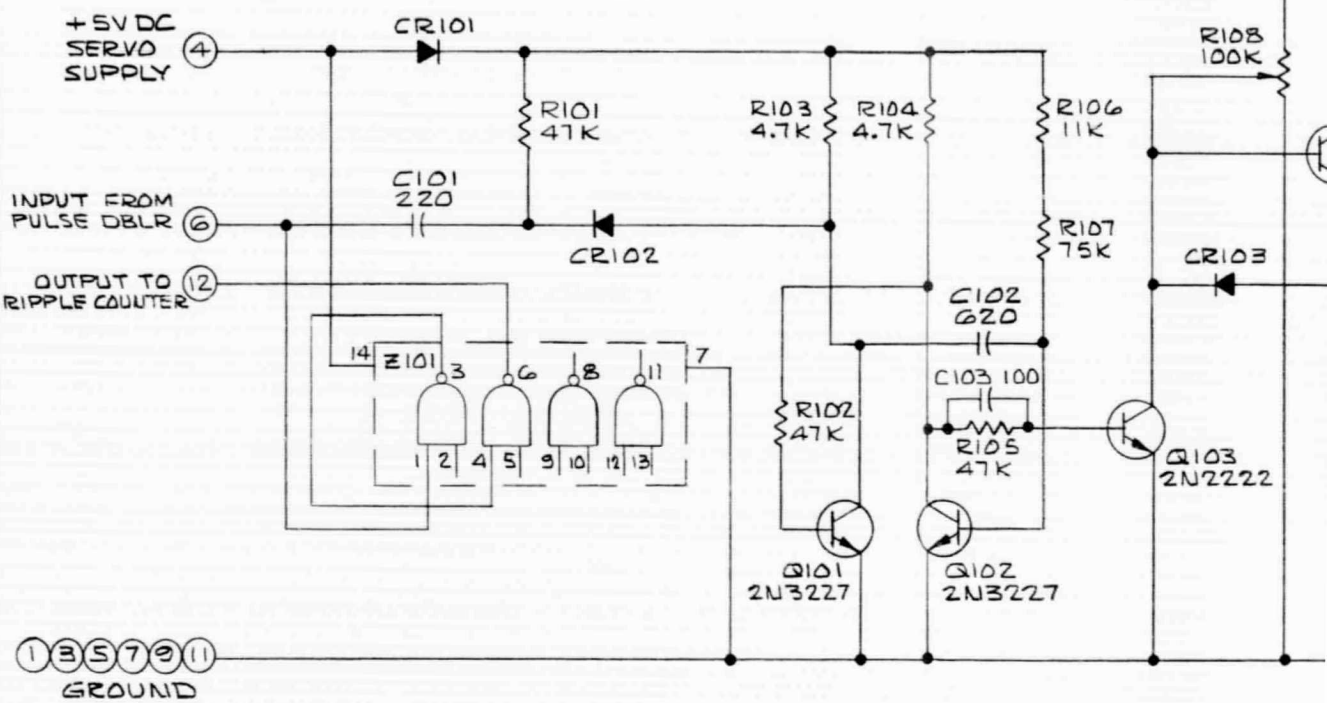
SCHEMATIC DATA & CLOCK INPUT BUFFERS

SCALE — DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS —
ANGLES — FRACTIONS —

BORG-WARNER CONTROLS
3300 SO. HALLADAY STREET
SANTA ANA, CALIFORNIA

DWG. C S-8072 CHG. B

C S-8072 B



5. SIGNAL CONDITIONING FUNCTION IS PERFORMED BY DTL946 GATE
4. Z101 IS FAIRCHILD DTL946
3. DIODES ARE IN914
2. CAPACITOR VALUES ARE IN PICOFARADS ±10% 200V
1. RESISTOR VALUES ARE IN OHMS ±5% 1/4 W

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT ASSY.	USED ON	PARTS LIST NO.
APPLICATION		

ITEM	REQ'D	PART NO.
		510 76094

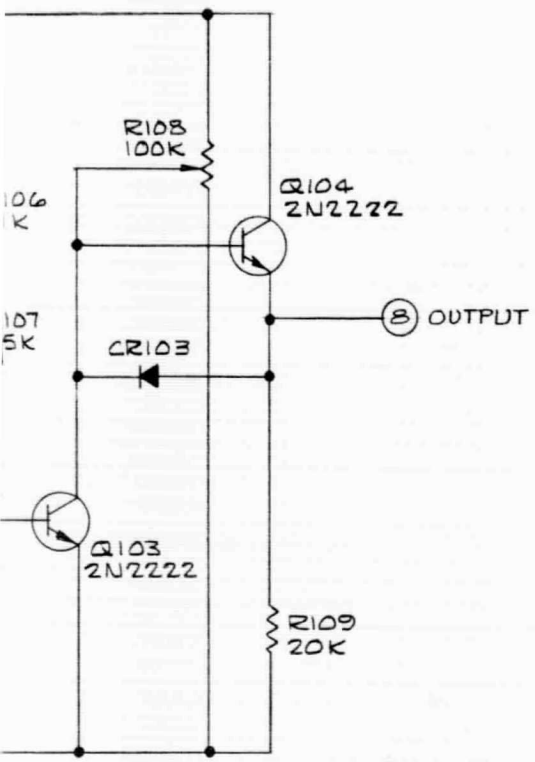
SPECIFICATIONS UNLESS OTHERWISE NOTED

ALL DIMENSIONS APPLY BEFORE ADDITIVE FIN
BREAK ALL EDGES AND SHARP CORNERS —— M
SURFACE ROUGHNESS √ MICRO INCH R.M.S. M
DIAMETERS TO BE CONCENTRIC WITHIN —— T.
FILLET RADIUS —— MAX.

DRAWN BY G. EVANS	DATE	3-13-
CHECKED BY	DATE	4-8-
DESIGN APP. R. Upshaw	DATE	4-6
PROJ. ENGR	DATE	

FOLDOUT FRAME 1

REVISIONS						
CHG.	ZONE	DESCRIPTION	E. C. O.	DATE	BY	CHKD
A		ADDED C103 & NOTE 5	—	4/4/68	GE	

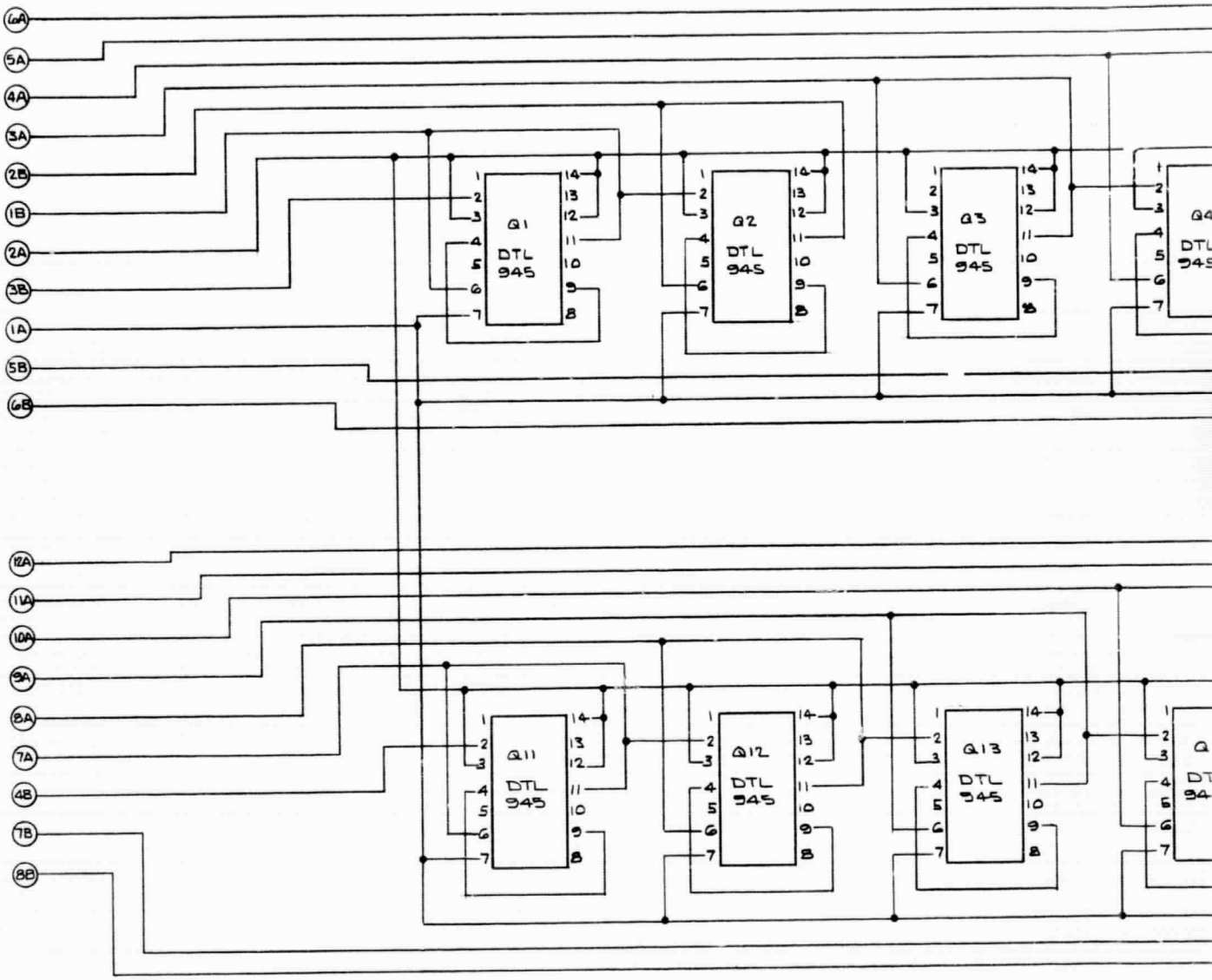


D'D	PART NO.	DESCRIPTION	MATERIAL	SPEC.	NOTE	SYMBOL
	76094	LIST OF MATERIALS				

ICATIONS UNLESS OTHERWISE NOTED SIONS APPLY BEFORE ADDITIVE FINISH EDGES AND SHARP CORNERS — MAX. OUGHNESS √ MICRO INCH R.M.S. MAX. TO BE CONCENTRIC WITHIN — T.I.R. IUS — MAX.	MATERIAL — HEAT TREATMENT —	SCHEMATIC FEEDBACK DISCRIMINATOR & GATE	BORG-WARNER CONTROLS 3300 SO. HALLADAY STREET SANTA ANA, CALIFORNIA	
a, EUDUS DATE 3-13-68 DATE 4-8-68 DATE 4-8-68 DATE	PROTECTIVE FINISH —	SCALE — DO NOT SCALE DRAWING UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS — ANGLES — FRACTIONS —	DWG. C S-8073	CHG. A

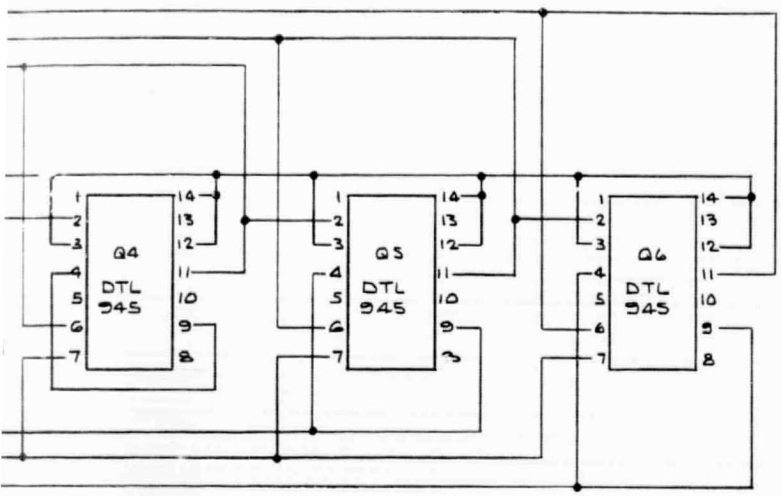
FOLDOUT FRAME 2

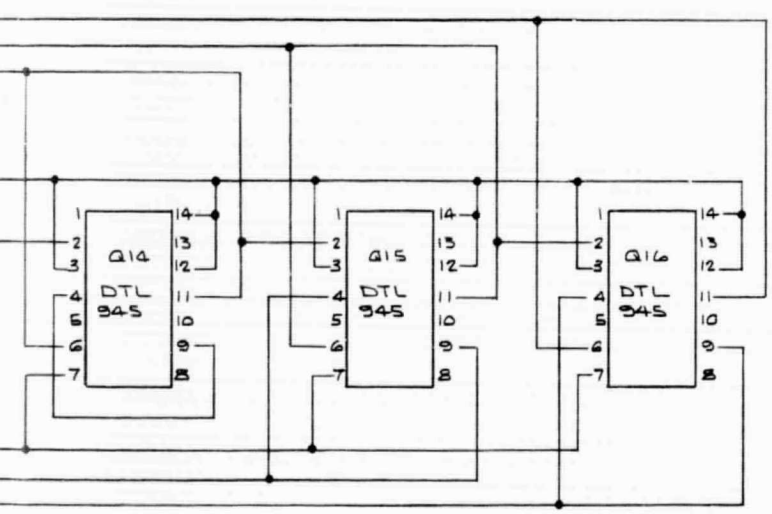
C-S-8073 A CHG.



4 3 2 1

REVISIONS					
CHG.	ZONE	DESCRIPTION	E. C. O.	DATE	BY	CHKD





ITEM	REQ'D	PART NO.	DESCRIPTION	MATERIAL	SPEC.	NOTE	SYMBOL

LIST OF MATERIALS

SPECIFICATIONS UNLESS OTHERWISE NOTED
ALL DIMENSIONS APPLY BEFORE ADDITIVE FINISH
BREAK ALL EDGES AND SHARP CORNERS [ ] MAX.
SURFACE ROUGHNESS ✓ MICRO INCH R.M.S. MAX.
DIAMETERS TO BE CONCENTRIC WITHIN [ ] T.I.R.
FILLET RADIUS [ ] MAX.

MATERIAL —
HEAT TREATMENT —
PROTECTIVE FINISH —

SCHEMATIC
RIPPLE COUNTER

BORG-WARNER CONTROLS
3300 SO. HALLADAY STREET
SANTA ANA, CALIFORNIA

DRAWN BY	G. EVANS	DATE 4-4-68
CHECKED BY		DATE 4-8-68
DESIGN APP.		DATE 4-8-68
PROJ. ENGR.		DATE

SCALE — DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS
ANGLES FRACTIONS

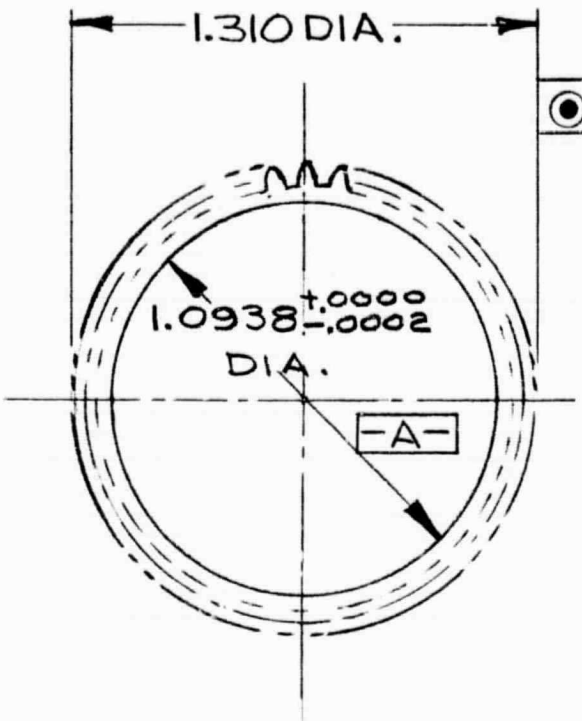
DWG. D S-8098 CHG.

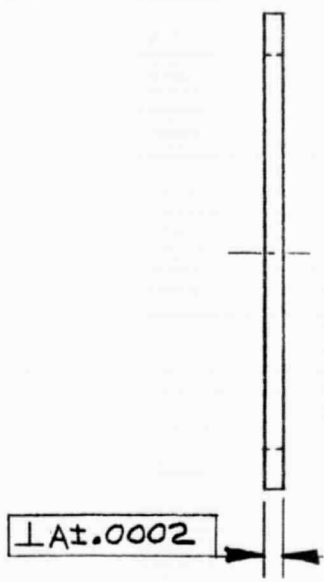
NEXT ASSY. | USED ON | PARTS LIST NO.
APPLICATION

FOLDOUT FRAME 2

5 4

D C B A





			ITEM	REQ'D	PART NO.	

SPECIFICATIONS UNLESS OTHERWISE NOTED

ALL DIMENSIONS APPLY BEFORE ADDITIVE FINISH

BREAK ALL EDGES AND SHARP CORNERS .005 MAX.

SURFACE ROUGHNESS 16 MICRO INCH R.M.S. MAX.

DIAMETERS TO BE CONCENTRIC WITHIN — T.I.R.

FILLET RADIUS — MAX.

MATERIAL S324 BOSTO

HEAT TREATM

PROTECTIVE

DRAWN BY	Phil Frost/ca.	DATE	4-4-68		
CHECKED BY		DATE	4-8-68		
DESIGN APP.	R Shpritzer	DATE	4-8-68		
PROJ. ENGR.		DATE			

NEXT ASSY.	USED ON	PARTS LIST NO.
APPLICATION		

FOLDOUT FRAME 1

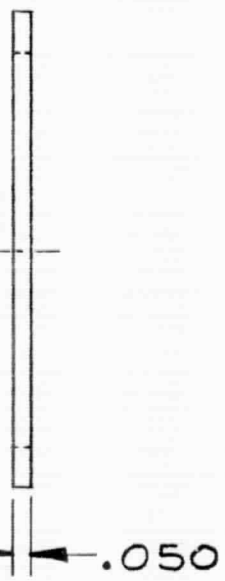
3 | B-S-8099 | CHG. 2 | 1

REVISIONS

CHG.	ZONE	DESCRIPTION	E. C. O.	DATE	BY	CHKD

D

C



B

DESCRIPTION	MATERIAL	SPEC.	NOTE	SYMBOL

LIST OF MATERIALS

A

RIAL
3240 GEAR
OSTON GEAR.

TREATMENT
NONE

ECTIVE FINISH
NONE

GEAR—TACHOMETER

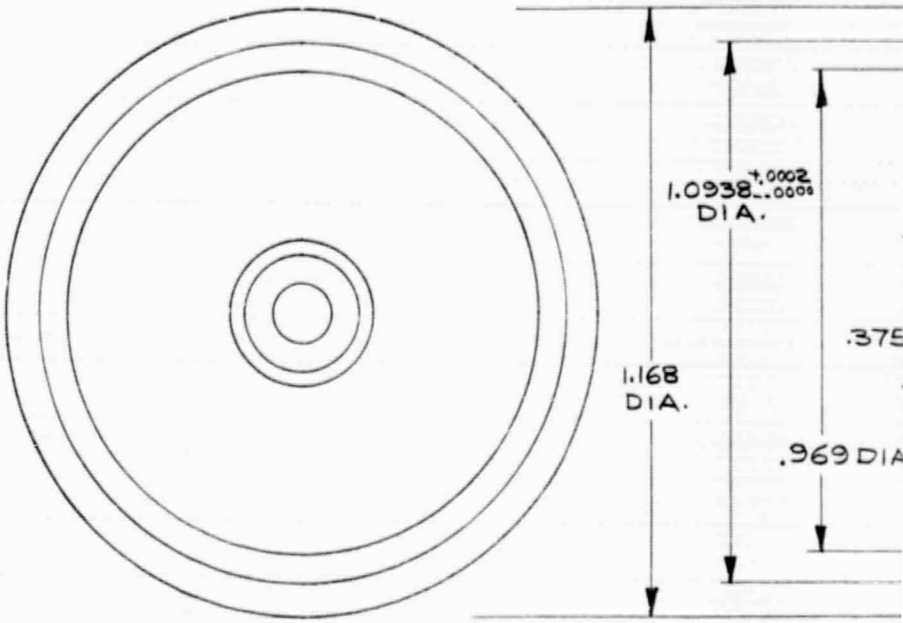
BORG-WARNER CONTROLS
3300 SO. HALLADAY STREET
SANTA ANA, CALIFORNIA

SCALE 2/1 | DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS .±.010
ANGLES — FRACTIONS —

DWG. B | S-8099 | CHG.

FOLDOUT FRAME 2



ITEM	REQ'D	PART NO.

SPECIFICATIONS UNLESS OTHERWISE

ALL DIMENSIONS APPLY BEFORE ADDI

BREAK ALL EDGES AND SHARP CORNER

SURFACE ROUGHNESS 32 MICRO INCH

DIAMETERS TO BE CONCENTRIC WITHIN

FILLET RADIUS .005 MAX.

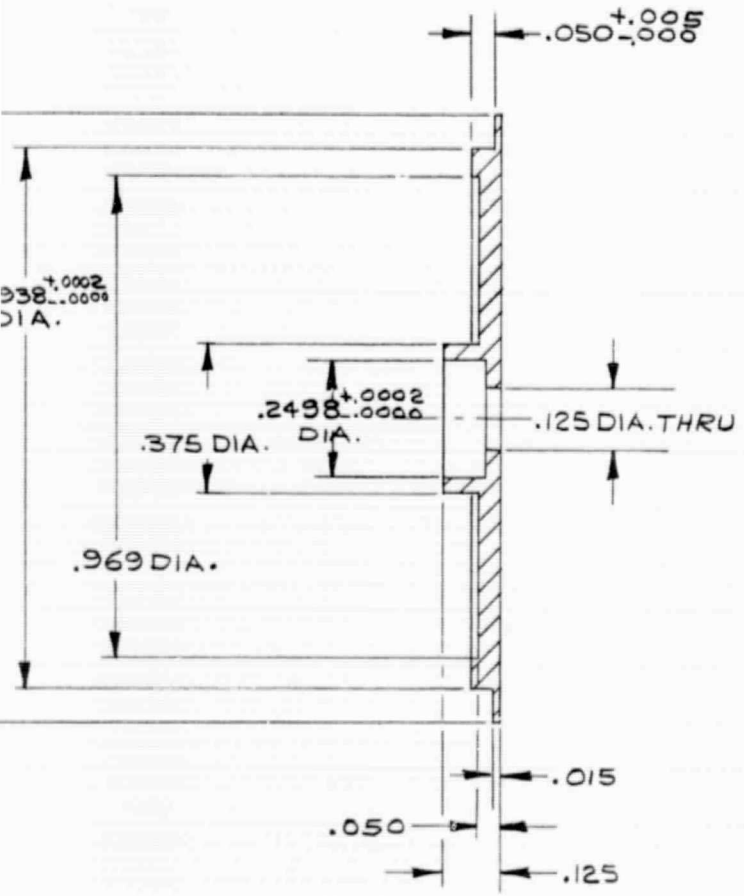
DRAWN BY	Phil Fanelli		DATE
CHECKED BY			DATE
DESIGN APP			DATE
PROJ. ENGR			DATE

NEXT ASSY.	USED ON	PARTS LIST NO.
APPLICATION		

FOLDOUT FRAME 1

2 1

REVISIONS					
CHG.	ZONE	DESCRIPTION	E. C. O.	DATE	BY / CHKD



D C B A

C-S-8100 CHG.

QTY	PART NO.	DESCRIPTION	MATERIAL	SPEC.	NOTE	SYMBOL

LIST OF MATERIALS

TOLERANCES UNLESS OTHERWISE NOTED
DIMENSIONS APPLY BEFORE ADDITIVE FINISH
SHARP EDGES AND SHARP CORNERS .005 MAX.
SURFACE ROUGHNESS 32 MICRO INCH R.M.S. MAX.
ALL SURFACES TO BE CONCENTRIC WITHIN .002 T.I.R.
RADIUS .005 MAX.

[illegible] Functional	DATE	4-4-68
[illegible]	DATE	4-4-68
[illegible] Approved	DATE	4-4-68
	DATE	

MATERIAL: 7075-T6 ALUM ALY PER QQ-A-225/9

HEAT TREATMENT: NONE

PROTECTIVE FINISH: NONE

HUB - TACH GEAR

SCALE 4/1 — DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS ±.005
ANGLES — FRACTIONS —

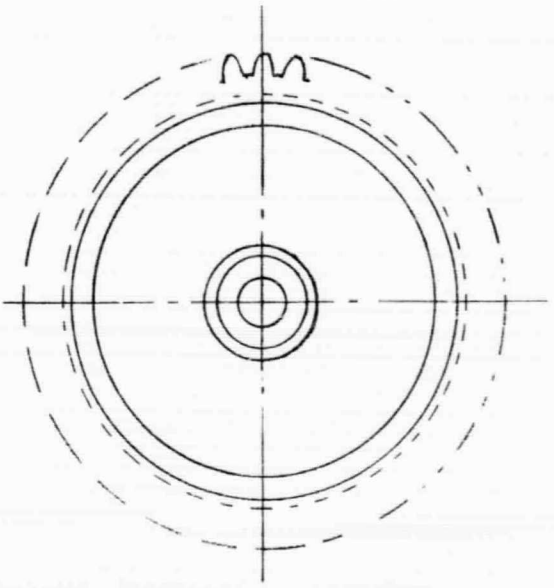
BORG-WARNER CONTROLS
3300 SO. HALLADAY STREET
SANTA ANA, CALIFORNIA

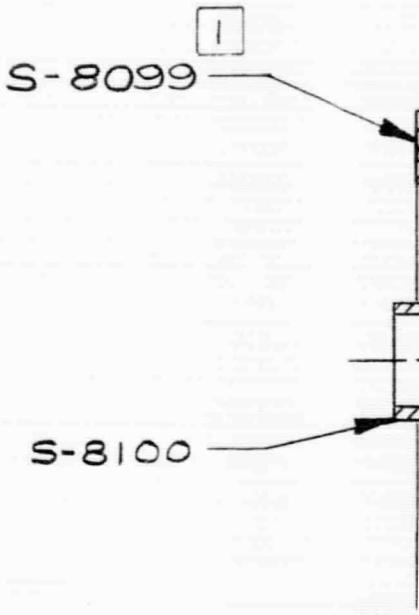
DWG. C S-8100 CHG.

FOLDOUT FRAME 2

5 4

D C B A





1 PRESS FIT S-8099 ON S-8100.

NOTES: UNLESS OTHERWISE SPECIFIED

ITEM	REQ'D	PART NO.	DES

SPECIFICATIONS UNLESS OTHERWISE NOTED

ALL DIMENSIONS APPLY BEFORE ADDITIVE FINISH

BREAK ALL EDGES AND SHARP CORNERS [—] MAX.

SURFACE ROUGHNESS √ MICRO INCH R.M.S. MAX.

DIAMETERS TO BE CONCENTRIC WITHIN [—] T.I.R.

FILLET RADIUS [—] MAX.

MATERIAL: No

HEAT TREATMENT: N

PROTECTIVE FINISH: N

DRAWN BY	Phil Frantz Jr.	DATE	4-5-68
CHECKED BY	[illegible]	DATE	4-8-68
DESIGN APP	[illegible]	DATE	4-8-68
PROJ. ENGR.		DATE	

NEXT ASSY.	USED ON	PARTS LIST NO.

APPLICATION

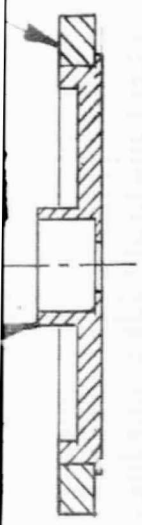
FOLDOUT FRAME 1

3 | B-S-8101 | CHG. 2 | 1

REVISIONS

CHG.	ZONE	DESCRIPTION	E. C. O.	DATE	BY	CHKD

D



C

B

DESCRIPTION	MATERIAL	SPEC.	NOTE	SYMBOL

LIST OF MATERIALS

NOTED

ENT
NONE

INISH
NONE

TACH GEAR ASS'Y

BORG-WARNER CONTROLS

3300 SO. HALLADAY STREET
SANTA ANA, CALIFORNIA

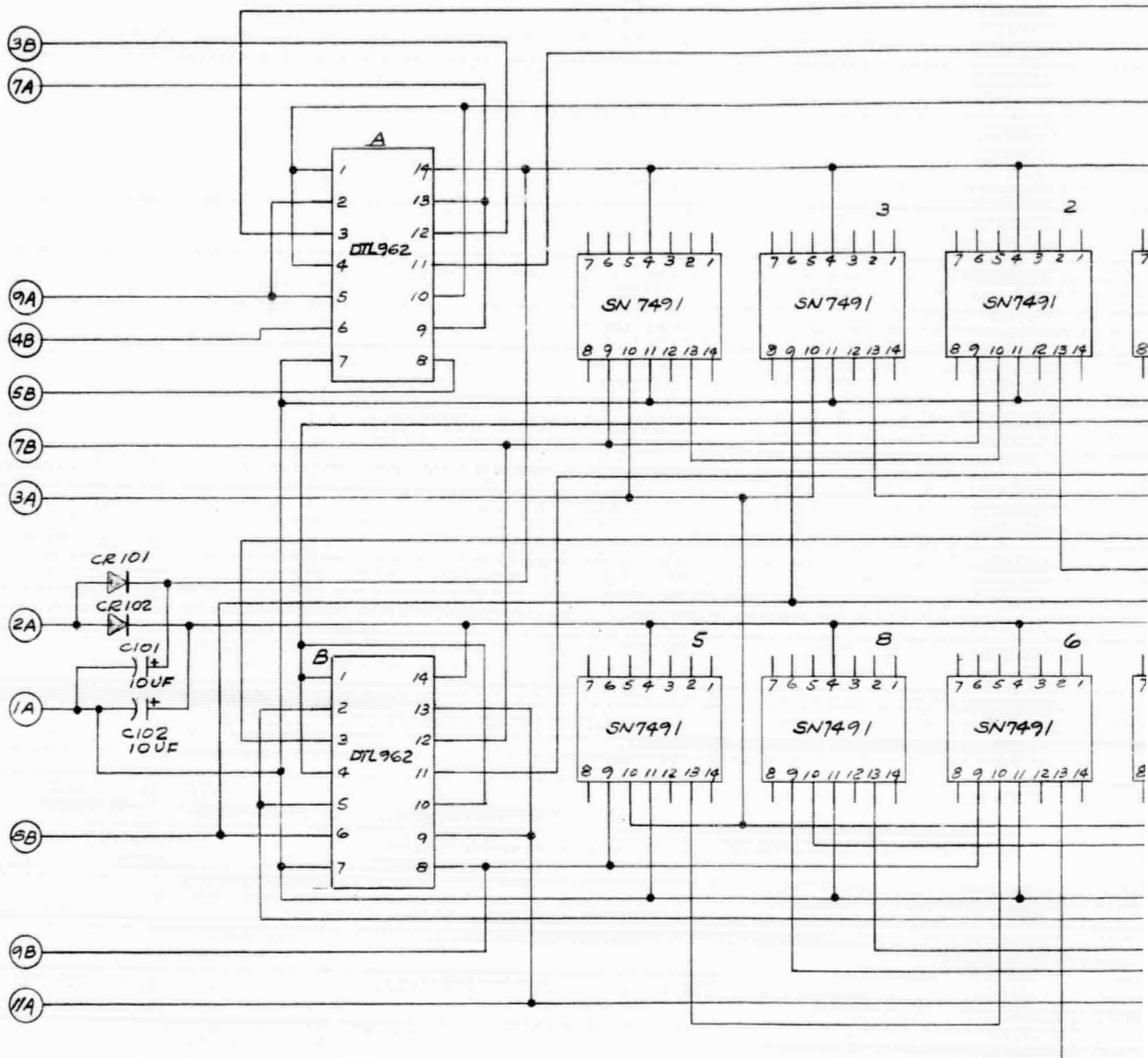
A

SCALE 2/1 | DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS —
ANGLES — FRACTIONS —

DWG. B | S-8101 | CHG.

FOLDOUT FRAME 2



[2] DIODES ARE TYPE IN914

[1] CAPACITOR VALUES ARE IN UF, 10V ± 10%

NOTES. UNLESS OTHERWISE SPECIFIED.

ITEM	REQ'D	PART NO.

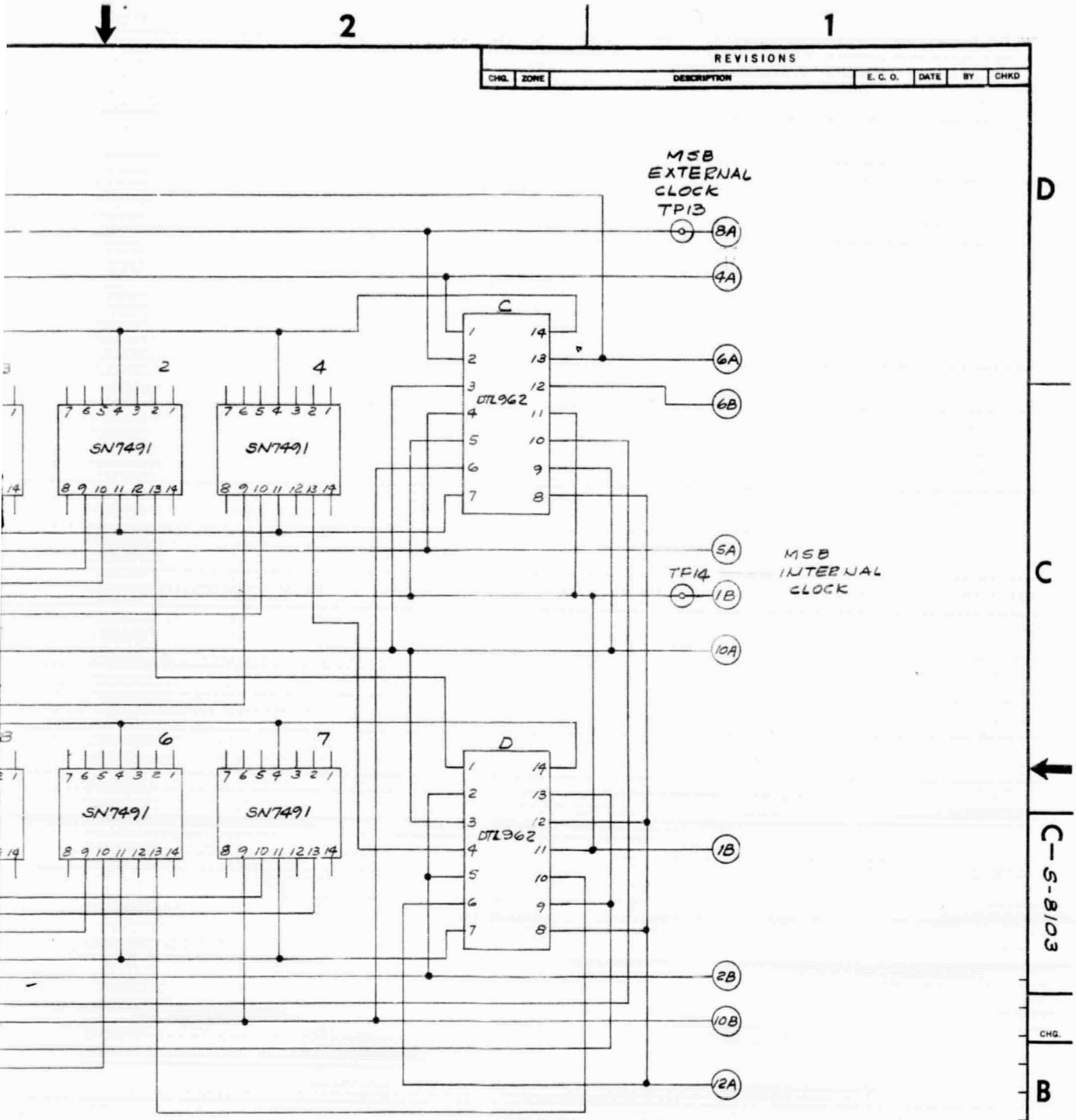
SPECIFICATIONS UNLESS OTHERWISE NOTED

ALL DIMENSIONS APPLY BEFORE ADDITIVE FINIS
BREAK ALL EDGES AND SHARP CORNERS — MA
SURFACE ROUGHNESS √ MICRO INCH R.M.S. MA
DIAMETERS TO BE CONCENTRIC WITHIN — T.I
FILLET RADIUS — MAX.

DRAWN BY RN.	DATE	4-4-68
CHECKED BY	DATE	4-8-68
DESIGN APP. R.H. Peters	DATE	4-8-68
PROJ. ENGR.	DATE	

NEXT ASSY.	USED ON	PARTS LIST NO.
APPLICATION		

FOLDOUT FRAME 1



REQ'D	PART NO.	DESCRIPTION	MATERIAL	SPEC.	NOTE	SYMBOL

LIST OF MATERIALS

SPECIFICATIONS UNLESS OTHERWISE NOTED
DIMENSIONS APPLY BEFORE ADDITIVE FINISH
ALL EDGES AND SHARP CORNERS — MAX.
SURFACE ROUGHNESS — MICRO INCH R.M.S. MAX.
HOLES TO BE CONCENTRIC WITHIN — T.I.R.
RADIUS — MAX.

MATERIAL

HEAT TREATMENT

PROTECTIVE FINISH

BUFFER REGISTER CARD

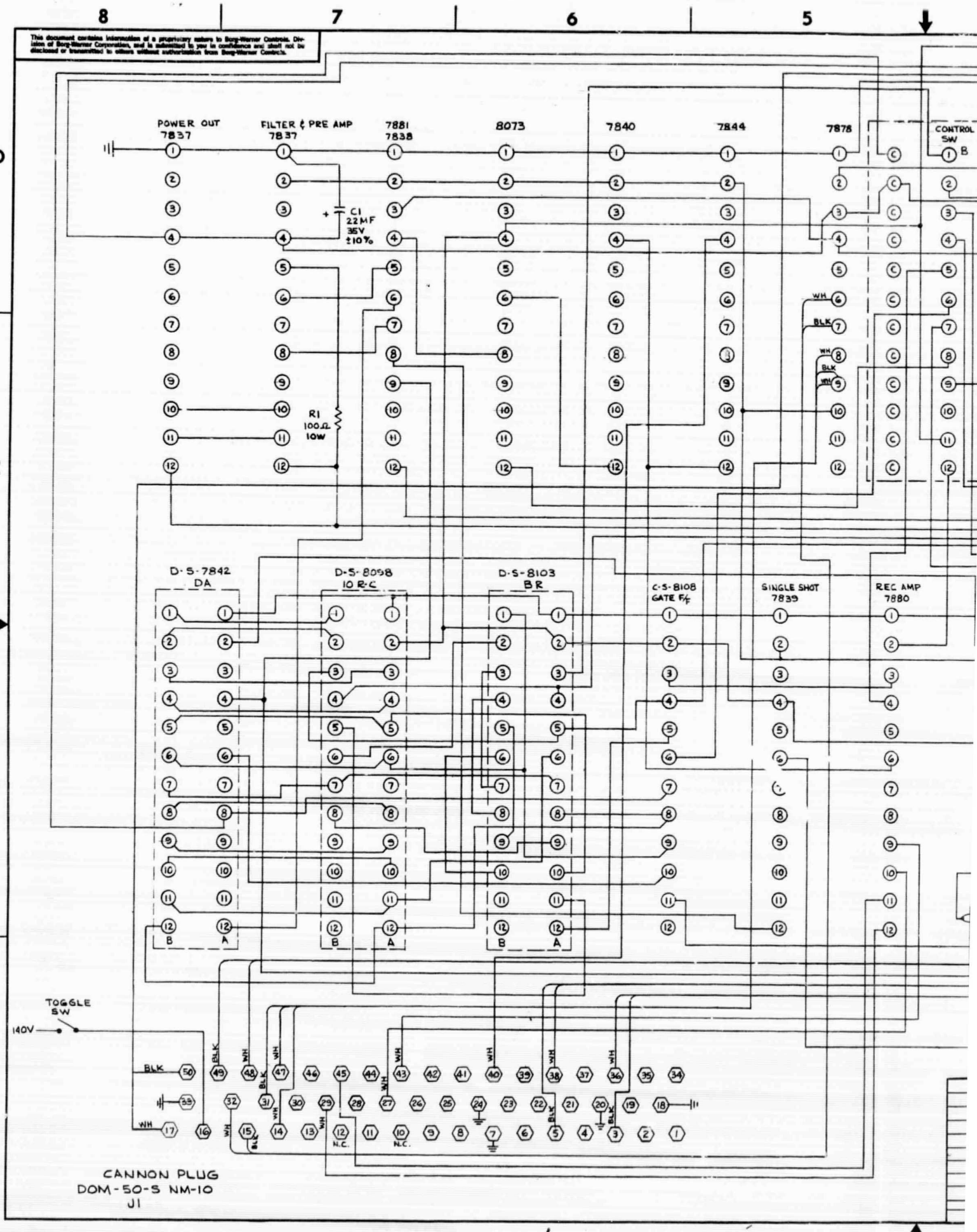
BORG-WARNER CONTROLS
3300 SO. HALLADAY STREET
SANTA ANA, CALIFORNIA

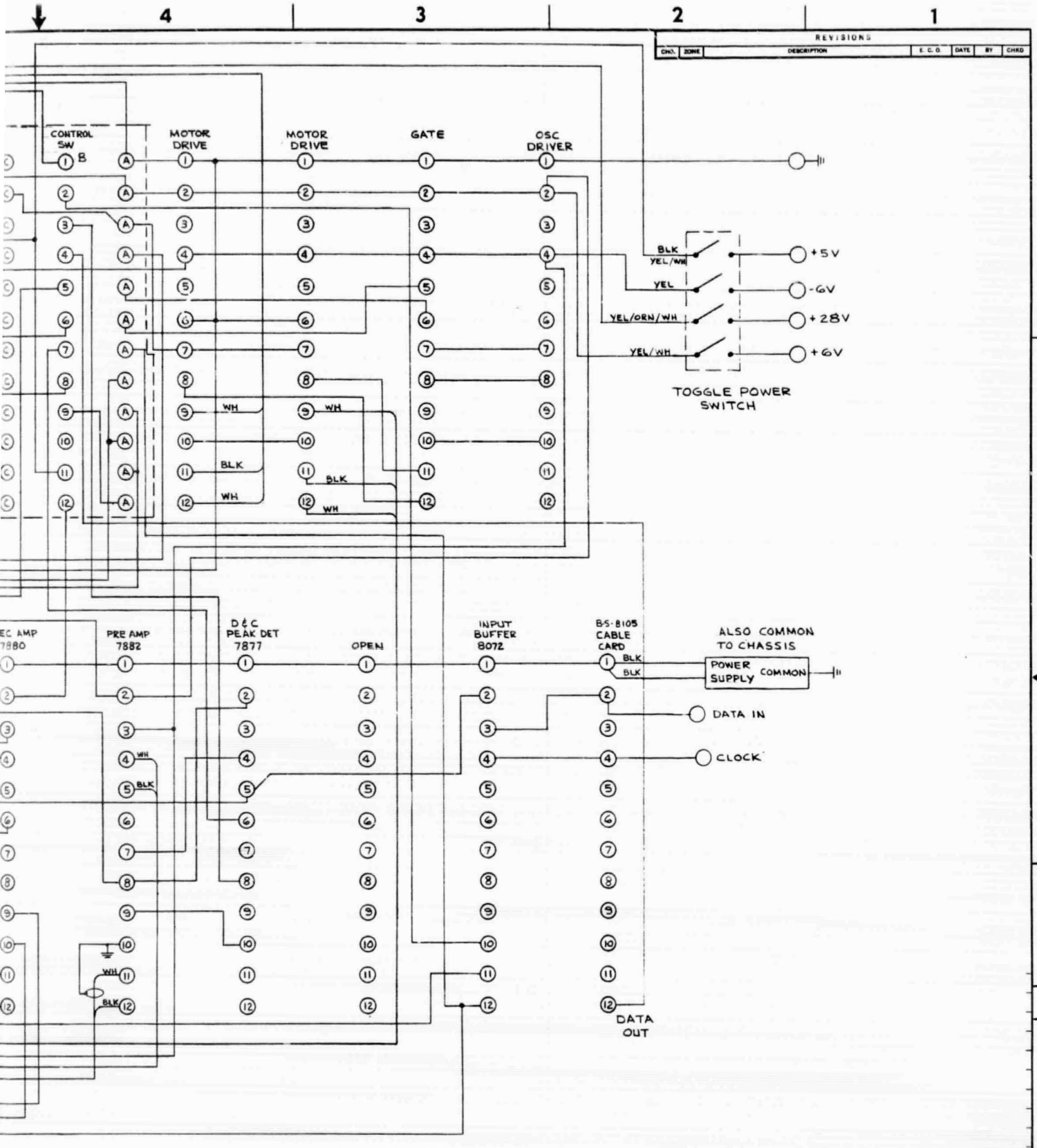
DRAWN BY	R.N.	DATE 4-4-68
CHKD BY	[illegible]	DATE 4-7-68
APP.	[illegible]	DATE 4-8-68
ENGR.		DATE

SCALE — DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS —
ANGLES — FRACTIONS —

DWG. C | S-8103 | CHG.

FOLDOUT FRAME 2





ITEM	REQ'D	PART NO.	DESCRIPTION	MATERIAL	SPEC.	NOTE	SYMBOL

LIST OF MATERIALS

SPECIFICATIONS UNLESS OTHERWISE NOTED
ALL DIMENSIONS APPLY BEFORE ADDITIVE FINISH
BREAK ALL EDGES AND SHARP CORNERS [ ] MAX.
SURFACE ROUGHNESS ✓ MICRO INCH R.M.S. MAX.
DIAMETERS TO BE CONCENTRIC WITHIN [ ] T.I.R.
FILLET RADIUS [ ] MAX.

MATERIAL
HEAT TREATMENT
PROTECTIVE FINISH

DRAWN BY W. SOUTAR DATE 4-9-68
CHECKED BY DM DATE 4-10-68
DESIGN APP. Dickstein DATE 4-10-68
PROJ. ENGR. DATE

CARD CAGE (REAR VIEW) INTERCONNECTION

SCALE ~ DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS
ANGLES FRACTIONS

BORG-WARNER CONTROLS
3300 SO. HALLADAY STREET
SANTA ANA, CALIFORNIA

DWG. D S-8104 CHG.

NEXT ASSY. | USED ON | PARTS LIST NO.
APPLICATION

FOLDOUT FRAME 2

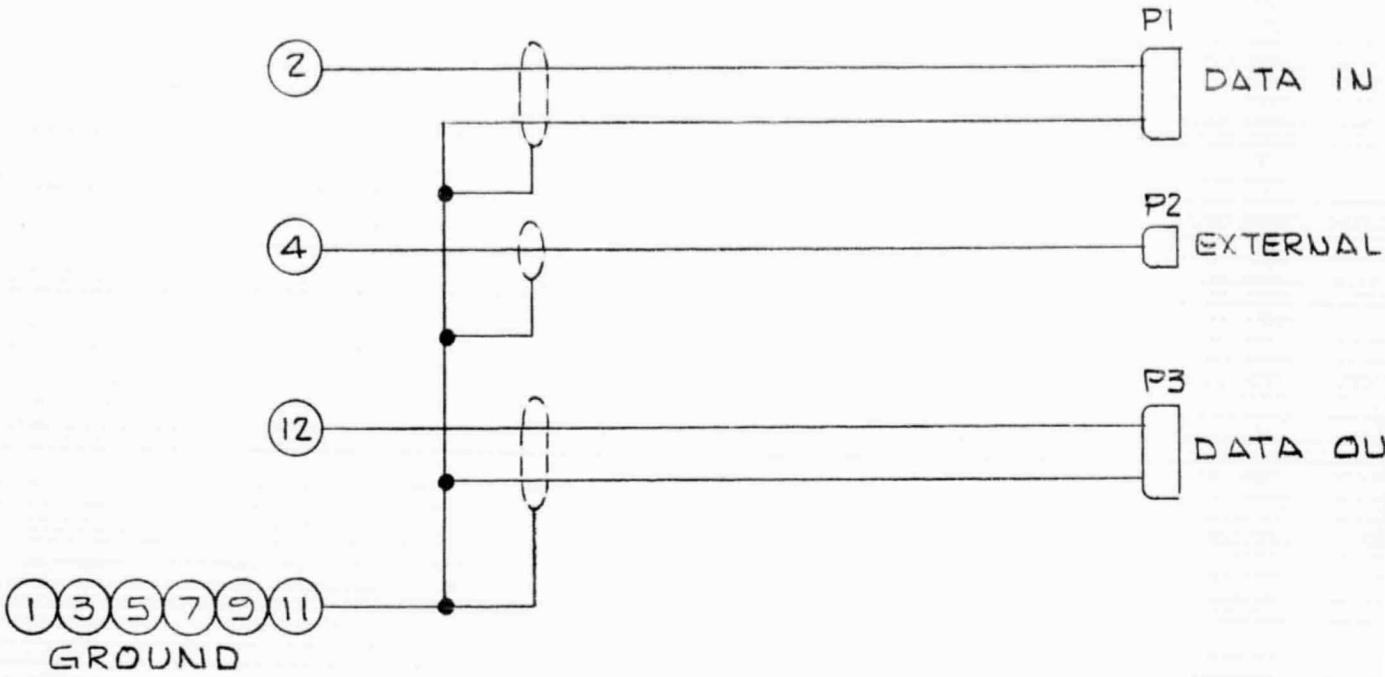
5 4 3

D

C

B

A



2. P3 IS BNC MALE PLUG
1. P1 & P3 ARE DUAL BANANA PLUGS

NOTES: UNLESS OTHERWISE SPECIFIED

ITEM	REQ'D	PART NO.	DESCRIPT

SPECIFICATIONS UNLESS OTHERWISE NOTED

ALL DIMENSIONS APPLY BEFORE ADDITIVE FINISH
BREAK ALL EDGES AND SHARP CORNERS [ ] MAX.
SURFACE ROUGHNESS ✓ MICRO INCH R.M.S. MAX.
DIAMETERS TO BE CONCENTRIC WITHIN [ ] T.I.R.
FILLET RADIUS [ ] MAX.

MATERIAL

HEAT TREATMENT

PROTECTIVE FINISH

DRAWN BY	G. EVANS	DATE	4-8-68
CHECKED BY	[illegible]	DATE	4-8-68
DESIGN APP.	[illegible]	DATE	4-8-68
PROJ. ENGR.		DATE	

NEXT ASSY.	USED ON	PARTS LIST NO.
APPLICATION		

3 | B– S-8105 | CHG. 2 | 1

REVISIONS

CHG.	ZONE	DESCRIPTION	E. C. O.	DATE	BY	CHKD

D

TA IN

ERNAL CLOCK

C

TA OUT

B

DESCRIPTION	MATERIAL	SPEC.	NOTE	SYMBOL

LIST OF MATERIALS

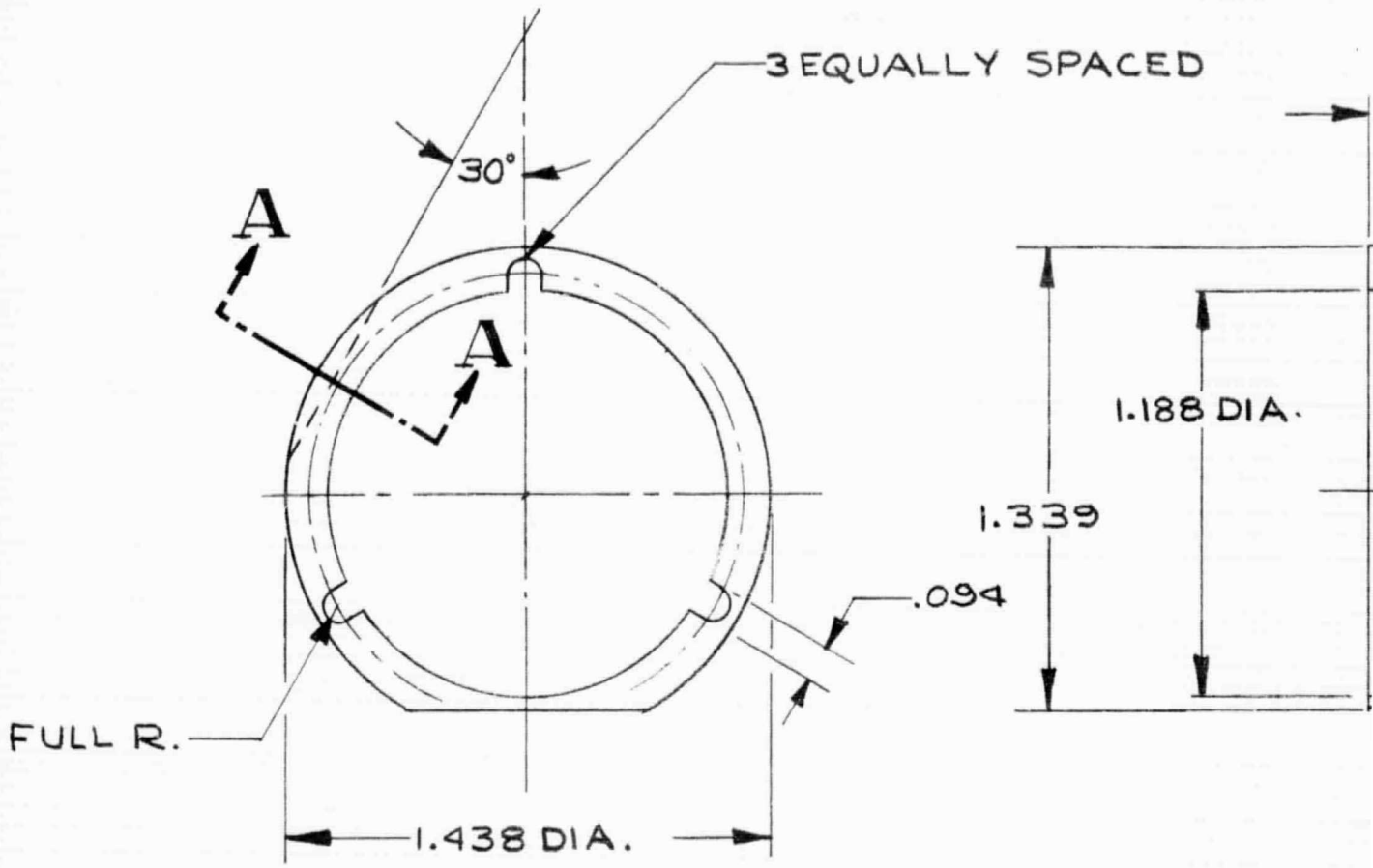
A

———	SCHEMATIC DATA AND CLOCK CABLES	BORG-WARNER CONTROLS 3300 SO. HALLADAY STREET SANTA ANA, CALIFORNIA
IENT ———		
FINISH ———	SCALE ——— DO NOT SCALE DRAWING UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS ANGLES FRACTIONS	DWG. B S-8105 CHG.

FOLDOUT FRAME 2

5 4 3

D C B A



ITEM	REQ'D	PART NO.	DESCRIP
		S/O 71012	

SPECIFICATIONS UNLESS OTHERWISE NOTED

ALL DIMENSIONS APPLY BEFORE ADDITIVE FINISH

BREAK ALL EDGES AND SHARP CORNERS .005 MAX.

SURFACE ROUGHNESS 63 MICRO INCH R.M.S. MAX.

DIAMETERS TO BE CONCENTRIC WITHIN .002 T.I.R.

FILLET RADIUS — MAX.

MATERIAL: 7075T6 AL PER QQA-2

HEAT TREATMENT: NO

PROTECTIVE FINISH: NOI

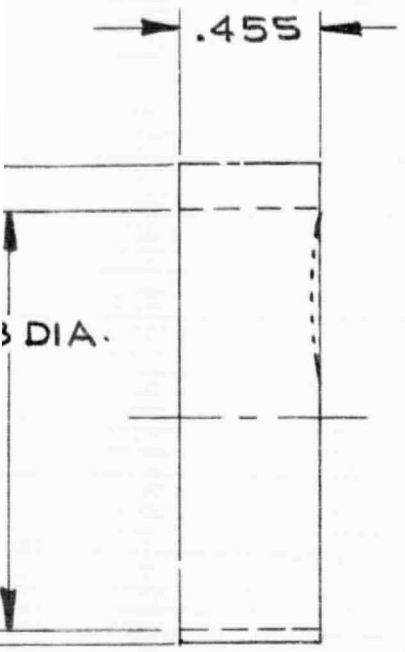
DRAWN BY	Phil Frasteja	DATE	4-8-68
CHECKED BY	[illegible]	DATE	4-8-68
DESIGN APP.	[illegible]	DATE	4-8-68
PROJ. ENGR.		DATE	

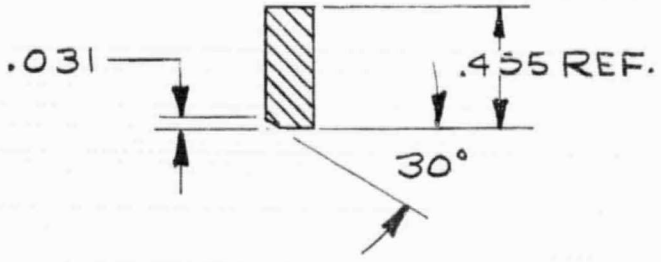
NEXT ASSY.	USED ON	PARTS LIST NO.
APPLICATION		

FOLDOUT FRAME 1

3 | B- S-8106 | CHG. 2 | 1

REVISIONS						
CHG.	ZONE	DESCRIPTION	E. C. O.	DATE	BY	CHKD





SECTION A-A
CHAMFER DETAIL

DESCRIPTION	MATERIAL	SPEC.	NOTE	SYMBOL

LIST OF MATERIALS

RIAL
75T6 ALUM ALLY
R QQA-225/9

TREATMENT
NONE

CTIVE FINISH
NONE

SPACER

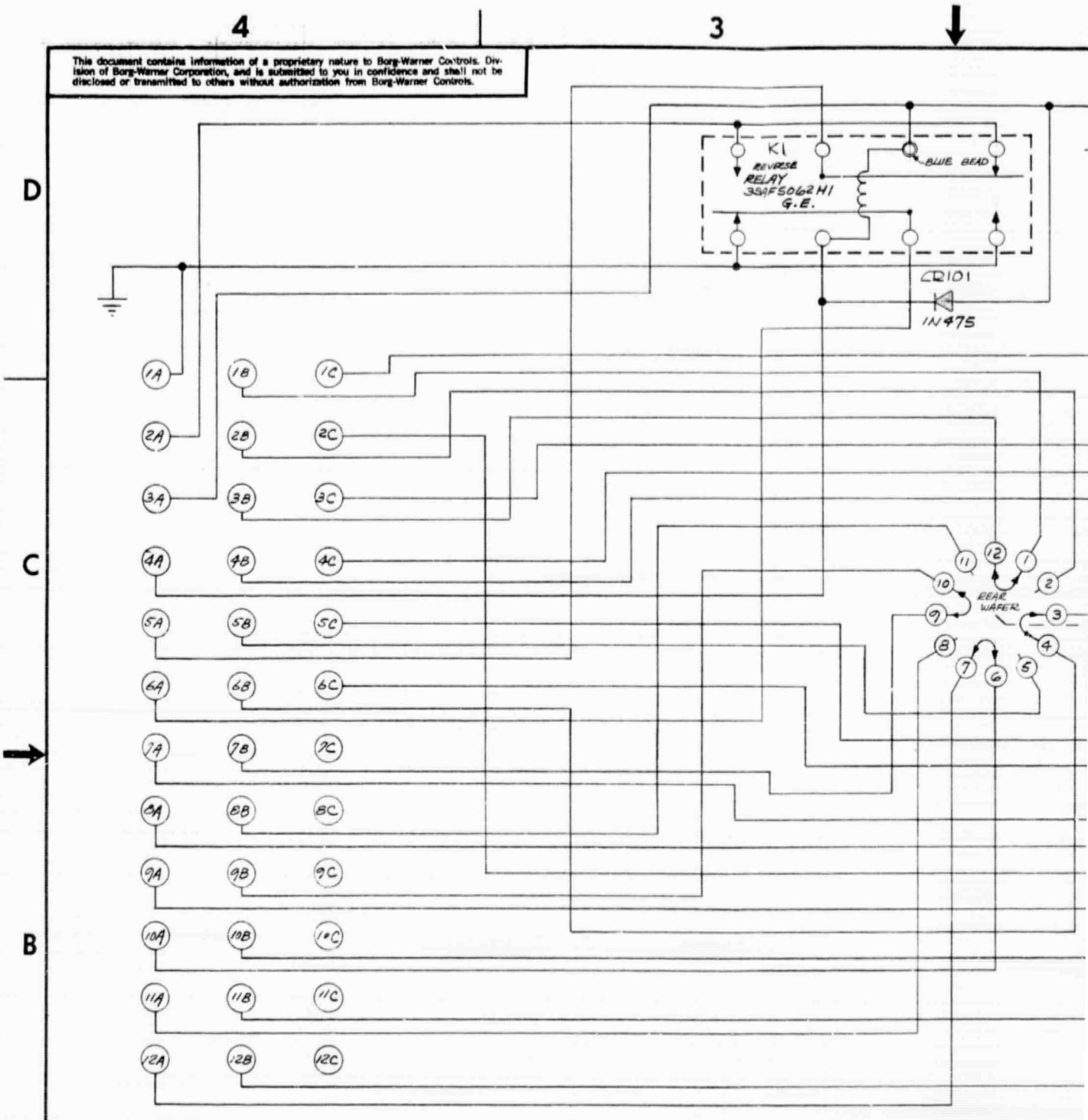
BORG-WARNER CONTROLS
3300 SO. HALLADAY STREET
SANTA ANA, CALIFORNIA

SCALE 2/1 | DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS ±.010
ANGLES ± 1° FRACTIONS —

DWG. B | S-8106 | CHG.

FOLDOUT FRAME 2



ITEM	REQ'D	PART NO.	

SPECIFICATIONS UNLESS OTHERWISE NOTED

ALL DIMENSIONS APPLY BEFORE ADDITIVE FINISH

BREAK ALL EDGES AND SHARP CORNERS — MAX.

SURFACE ROUGHNESS — MICRO INCH R.M.S. MAX.

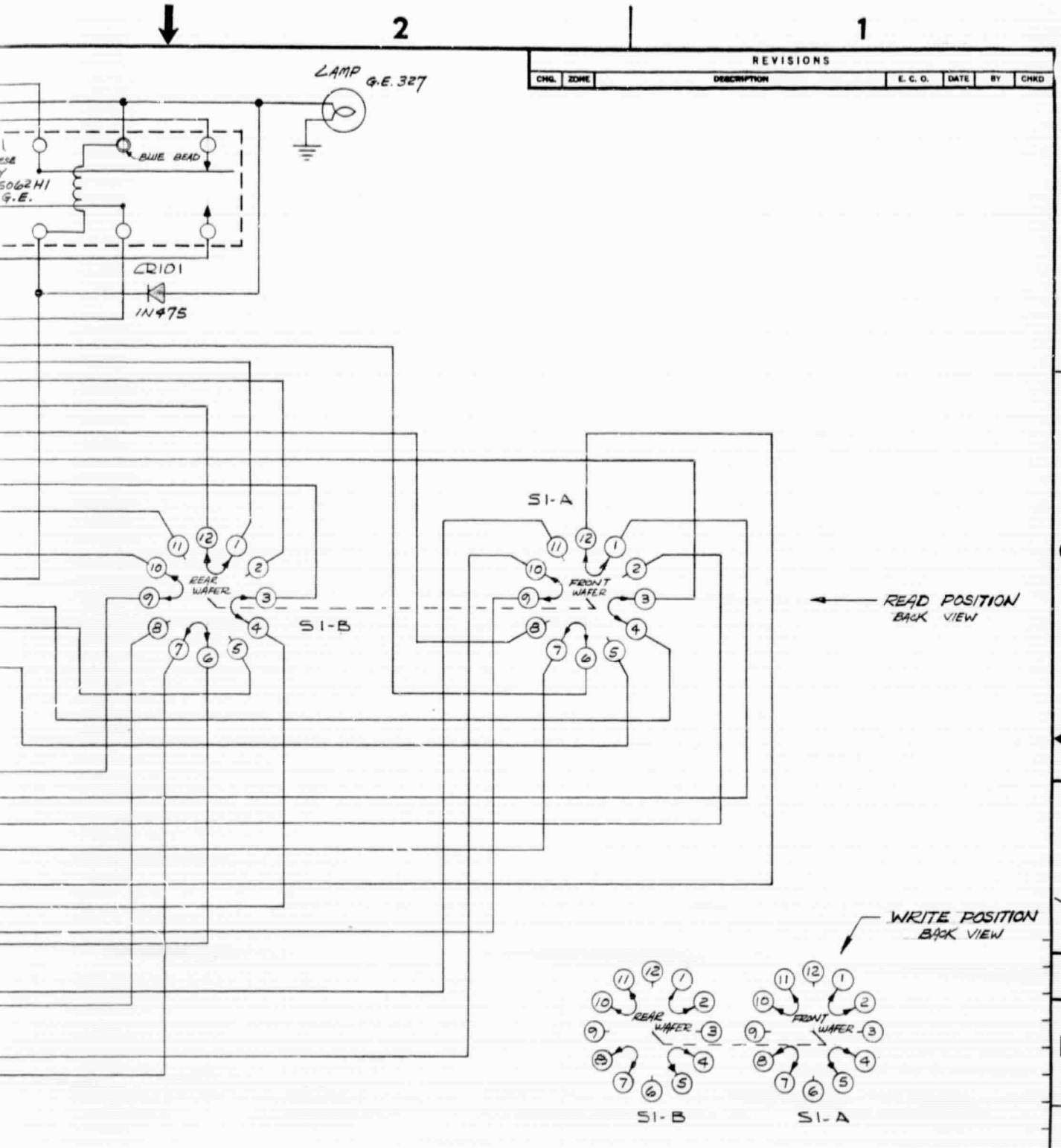
DIAMETERS TO BE CONCENTRIC WITHIN — T.I.R.

FILLET RADIUS — MAX.

DRAWN BY	R N	DATE	4-8-68
CHECKED BY		DATE	4-9-68
DESIGN APP.		DATE	4-9-68
PROJ. ENGR.		DATE	

NEXT ASSY.	USED ON	PARTS LIST NO.
	APPLICATION	

FOLDOUT FRAME 1



ITEM	REQ'D	PART NO.	DESCRIPTION	MATERIAL	SPEC.	NOTE	SYMBOL

LIST OF MATERIALS

SPECIFICATIONS UNLESS OTHERWISE NOTED
ALL DIMENSIONS APPLY BEFORE ADDITIVE FINISH
BREAK ALL EDGES AND SHARP CORNERS ___ MAX.
SURFACE ROUGHNESS √ MICRO INCH R.M.S. MAX.
DIAMETERS TO BE CONCENTRIC WITHIN ___ T.I.R.
FILLET RADIUS ___ MAX.

MATERIAL

HEAT TREATMENT

PROTECTIVE FINISH

SCHEMATIC
CONTROL SW. CARD

BORG-WARNER CONTROLS
3300 SO. HALLADAY STREET
SANTA ANA, CALIFORNIA

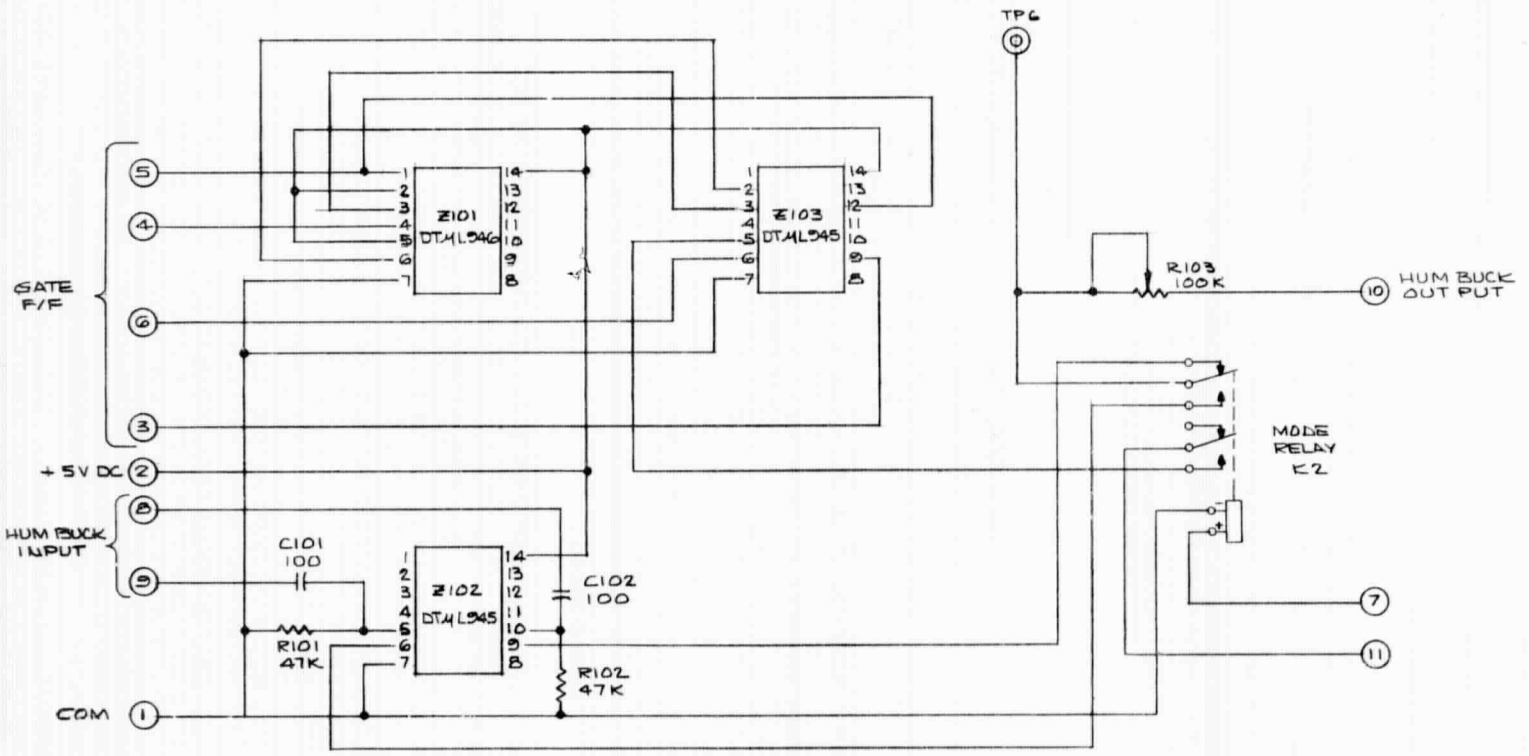
DRAWN BY	R N	DATE 4-8-68
CHECKED BY	[illegible]	DATE 4-9-68
DESIGN APP.	[illegible]	DATE 4-9-68
PROJ. ENGR.		DATE

SCALE ___ DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS
ANGLES FRACTIONS

DWG. C | S-8107 | CHG.

FOLDOUT FRAME 2

REVISIONS						
CHG.	ZONE	DESCRIPTION	E.C.O.	DATE	BY	CHKD
A		TERM # 11 WAS # 4	—	4/6/68	CR	



2. CAPACITOR VALUES ARE IN PICOFARADS ±10% 200V

1. RESISTOR VALUES ARE IN OHMS ± 5% 1/4W

NOTES: UNLESS OTHERWISE SPECIFIED

ITEM	REQ'D	PART NO.	DESCRIPTION	MATERIAL	SPEC.	NOTE	SYMBOL

LIST OF MATERIALS

NEXT ASSY.	USED ON	PARTS LIST NO.
APPLICATION		

SPECIFICATIONS UNLESS OTHERWISE NOTED
ALL DIMENSIONS APPLY BEFORE ADDITIVE FINISH
BREAK ALL EDGES AND SHARP CORNERS ☐ MAX.
SURFACE ROUGHNESS ✓ MICRO INCH R.M.S. MAX.
DIAMETERS TO BE CONCENTRIC WITHIN ☐ T.I.R.
FILLET RADIUS ☐ MAX.

DRAWN BY	G. EVANS	DATE 4-8-68
CHECKED BY		DATE 4-9-68
DESIGN APP.		DATE 4-9-68
PROJ. ENGR.		DATE

MATERIAL —
HEAT TREATMENT —
PROTECTIVE FINISH —

SCHEMATIC
GATE FLIP FLOP
HUM BUCK F/F
& MODE RELAY

SCALE — DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS
ANGLES FRACTIONS

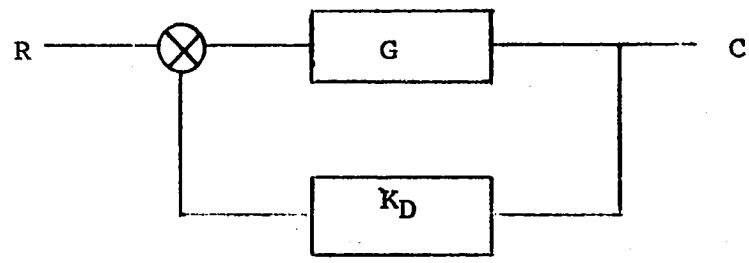
BORG-WARNER CONTROLS
3300 SO. HALLADAY STREET
SANTA ANA, CALIFORNIA

DWG. C S-8108 CHG. A

APPENDIX A

CONTINUOUSLY-ADJUSTABLE, VARIABLE-SPEED, PHASE LOCK SERVO SYSTEM

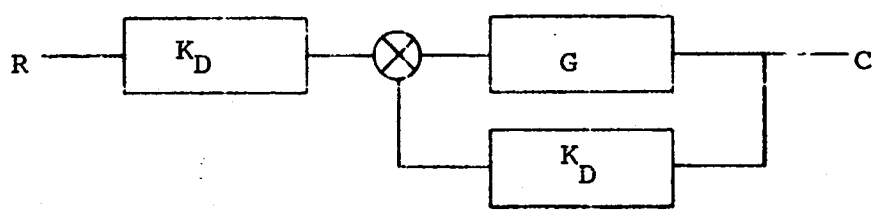
I. Consider the inner loop only (of a double-loop, phase-lock servo).



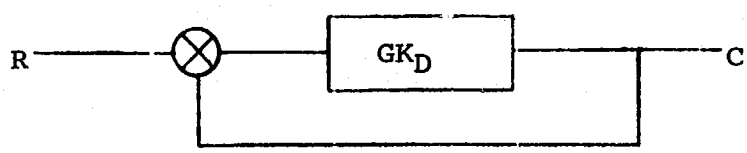
$$\frac{C}{R} = \frac{G}{1 + GK_D} \quad \text{for } GK_D \gg 1$$

$$\frac{C}{R} = \frac{1}{K_D}$$

If a second discriminator is added ahead of the closed loop



By block diagram transformation

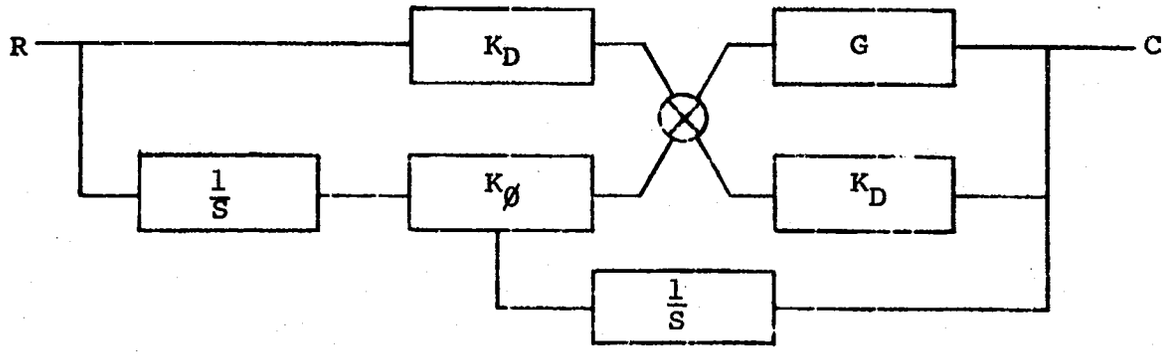


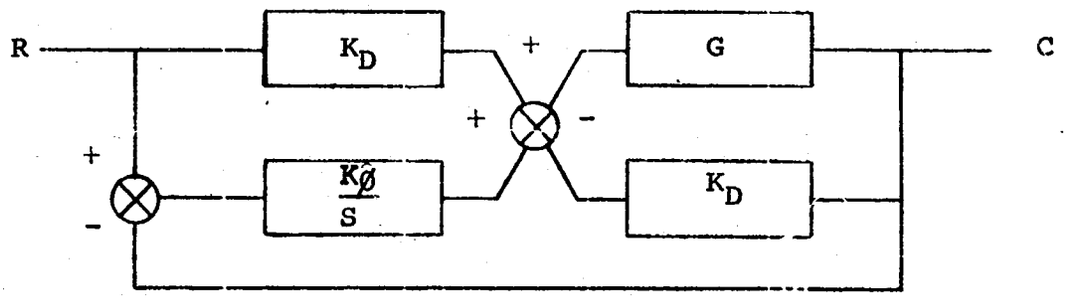
$$\frac{C}{R} = \frac{GK_D}{1 + GK_D}$$

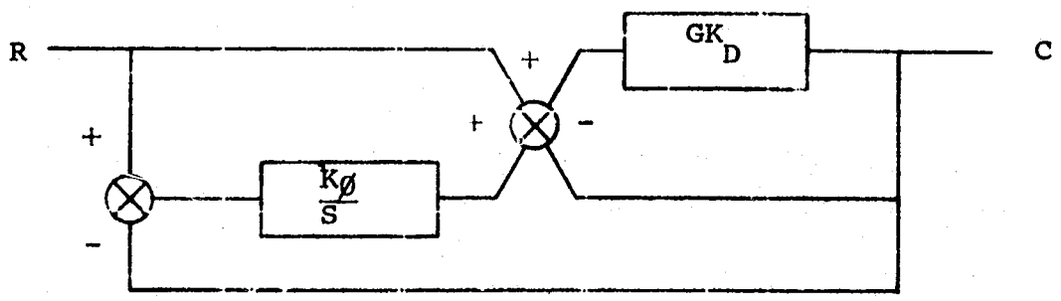
again for $GK_D \gg 1 \quad \frac{C}{R} = 1$

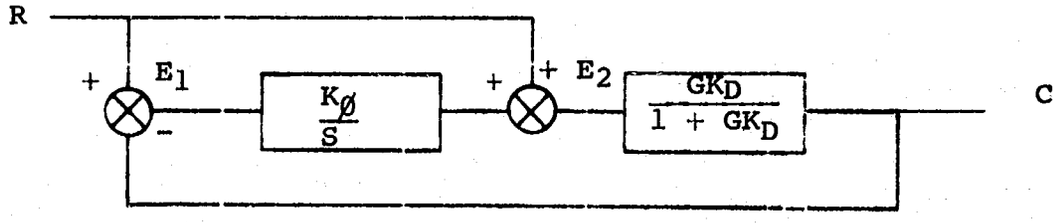
Thus the output frequency is slaved to the input frequency, but not with zero error as in the phase-lock loop.

II. Phase-lock loop added to the foregoing.









The latter diagram is as simplified as possible.

$$E_1 = R - C \qquad E_2 = R + \frac{K_\phi}{S}(E_1)$$

$$\frac{C}{E_2} = \frac{GK_D}{1 + GK_D}$$

$$C = \frac{GK_D}{1 + GK_D}\left(R + \frac{K_\phi}{S} E_1\right)$$

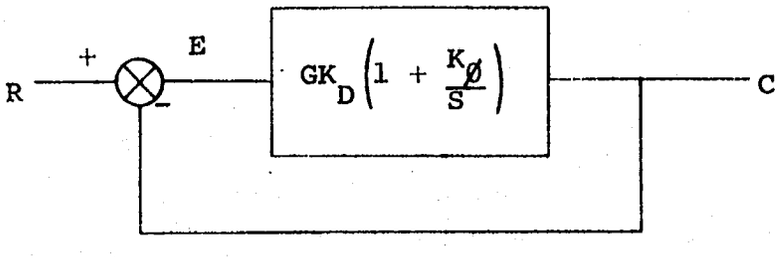
$$C = \frac{GK_D}{1 + GK_D}\left[R + \frac{K_\phi}{S}(R - C)\right]$$

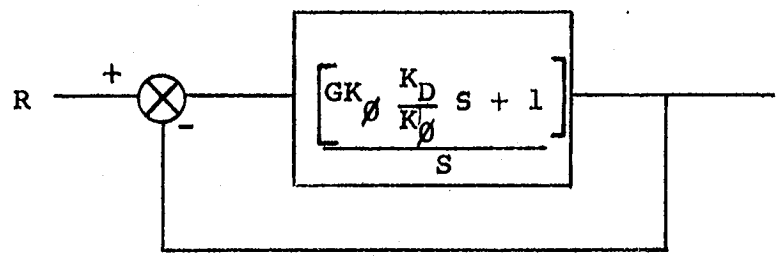
$$(1 + GK_D)C = GK_D R + \frac{K_\phi}{S} GK_D R - \frac{GK_D K_\phi}{S} C$$

$$\left(1 + GK_D + \frac{GK_D K_\phi}{S}\right)C = R\left(GK_D + \frac{K_\phi}{S} GK_D\right)$$

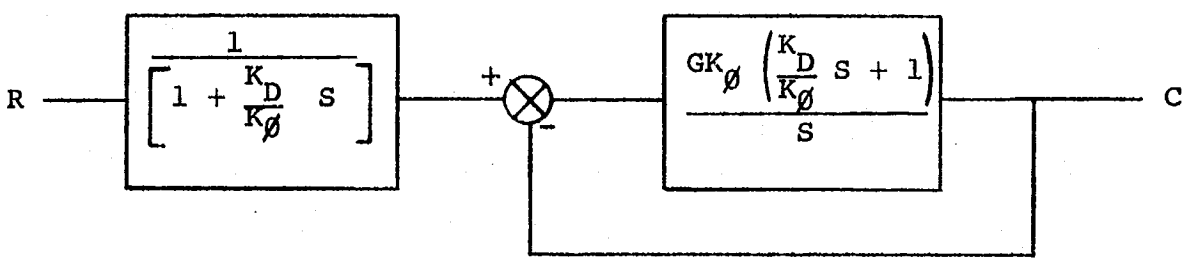
$$\frac{C}{R} = \frac{GK_D\left(1 + \frac{K_\phi}{S}\right)}{1 + GK_D\left(1 + \frac{K_\phi}{S}\right)}$$

Thus, the equivalent block diagram is





This compares with the diagram below for a conventional double loop system without a feed-forward discriminator.



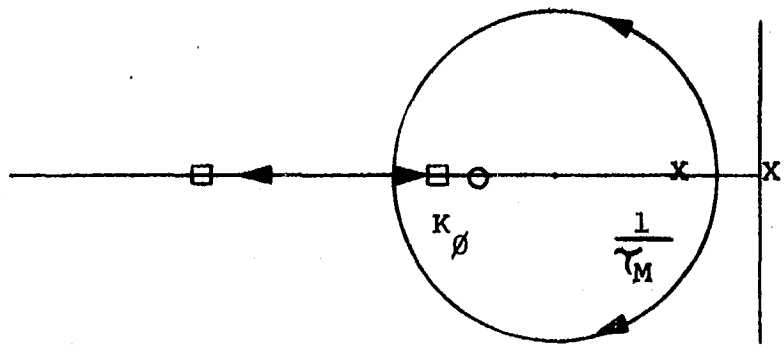
This equivalent open-loop transfer function

$$\frac{C}{E} = GK_D \left(1 + \frac{K_\phi}{S}\right) = GK_D \left(\frac{S + K_\phi}{S}\right) = GK_D K_\phi \left(\frac{1 + \frac{S}{K_\phi}}{S}\right)$$

can be analyzed for closed-loop stability, etc., for various G, using root locus and/or frequency response methods.

$$\frac{C}{E} = \frac{GK_D}{S}\left(S + K_\phi\right) = \frac{GK_DK_\phi}{\quad}\left(\quad + 1\right)$$

for $$G = \frac{K_M}{(\tau_M S + 1)}$$



□ = Closed Loop Pole

X = Open Loop Pole

O = Zero

Thus, without compensation a stable system is achievable, although static error and other characteristics may not be acceptable. If they are acceptable, G can be modified to include equalization, offering better overall characteristics.

APPENDIX B

MULTI SPEED SERVO ACTIVE RIPPLE FILTER

Design for transitional Butterworth/Thompson.

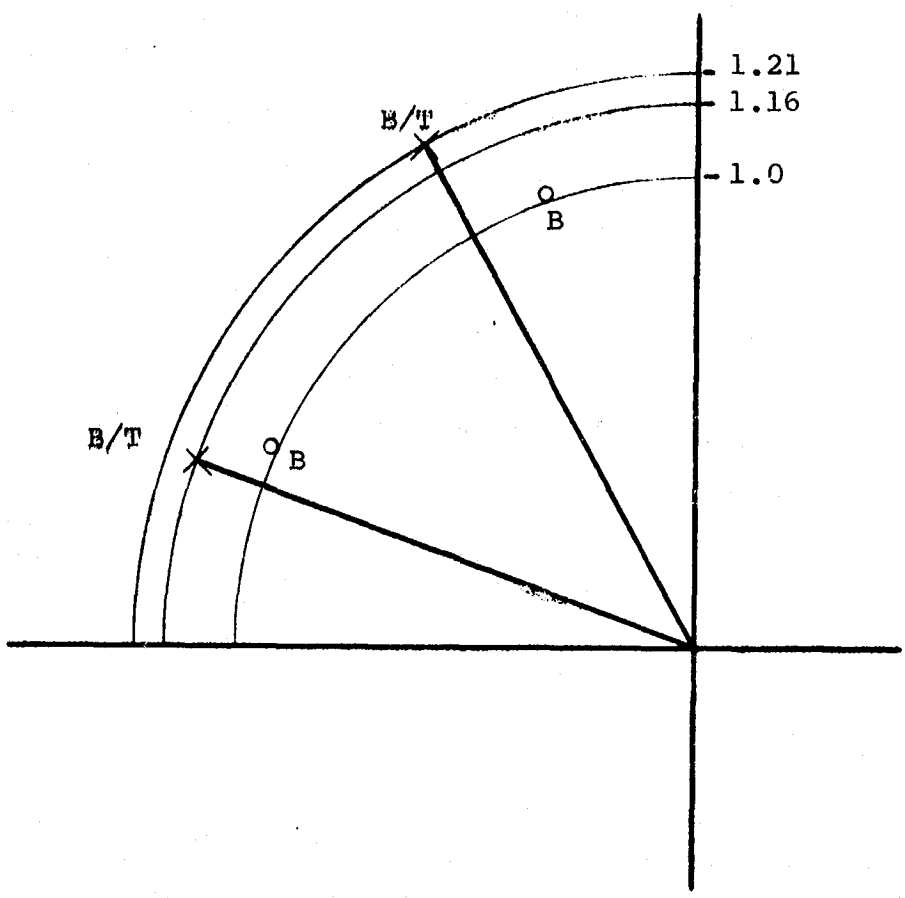
$S_{1,2} = -1.0858 \pm j.3987$ $\quad \tan^{-1} 0.367 = \phi = 20°10'$

$\cos\phi = \zeta = 0.938$

$S_{3,4} = -0.5843 \pm j1.0605$ $\quad \tan^{-1} 1.818 = \phi = 61°10'$

$\cos\phi = \zeta = 0.483$

200 Hz Butterworth/Thompson LPF:



Set poles at 242 Hz $\zeta = 0.483$

232 Hz $\zeta = 0.938$

The closest Boonshaft and Fuchs slide rule points are:

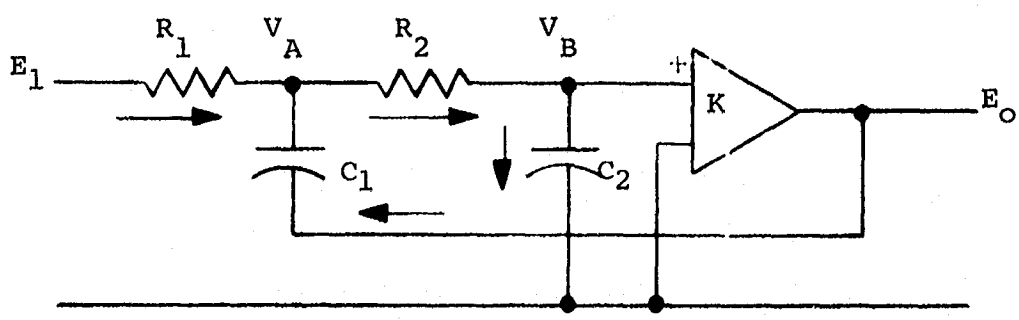
224 Hz ζ = 0.95

251 Hz ζ = 0.50

Hz	dB	$\angle$
10	0.0	- 7°
20	0.1	- 15°
32	0.0	- 22°
63	- 0.2	- 45°
79	- 0.5	- 57°
100	- 0.7	- 72°
159	- 1.9	
200	- 3.4	
251	- 6.6	-187°
398	-16.9	
631	-34.3	
1000	-50.0	

Using positive feedback, the active filter is derived from the current mode Kirchoff equations.

Assume $V_B = 0$



$$\frac{E_1 - V_A}{R_1} + \frac{E_o - V_A}{\frac{1}{C_1 S}} = \frac{V_A - V_B}{R_2} = \frac{V_B}{\frac{1}{C_2 S}} \qquad KV_B = E_o$$

$$\frac{E_1}{R_1} - \frac{V_A}{R_1} + C_1 S E_o - C_1 S V_A = \frac{V_A}{R_2} - \frac{E_o}{KR_2} = \frac{E_o}{K} \; C_2 S$$

$$V_A = R_2 \frac{E_o}{K} \left[C_2 S + \frac{1}{R_2} \right]$$

$$= \frac{E_o}{K} \left[R_2 C_2 S + 1 \right]$$

$$\frac{E_1}{R_1} + C_1 S E_o - V_A \left(C_1 S + \frac{1}{R_1} \right) = \frac{E_o C_2 S}{K}$$

$$\frac{E_1}{R_1} + C_1 S E_o - \frac{E_o}{K} \left(R_2 C_2 S + 1 \right) \left(C_1 S + \frac{1}{R_1} \right) = \frac{E_o C_2 S}{K}$$

$$\frac{E_1}{R_1} = \frac{E_o}{K} \left[\left(R_2 C_2 S + 1 \right) \left(C_1 S + \frac{1}{R} \right) + C_2 S - C_1 S K \right]$$

$$\frac{E_o}{E_1} = \frac{K}{R_1} \; \frac{1}{\left(R_2 C_2 S + 1 \right) \left(C_1 S + \frac{1}{R_1} \right) + \left(C_2 - C_1 K \right) S}$$

$$= \frac{K}{\left(R_2 C_2 S + 1 \right) \left(R_1 C_1 S + 1 \right) + R_1 \left(C_2 - C_1 K \right) S}$$

$$= \frac{K}{R_2 C_2 R_1 C_1 S^2 + \left(R_1 C_1 + R_2 C_2 + R_1 C_2 - K R_1 C_1 \right) S + 1}$$

$$= \frac{K}{R_2 C_2 R_1 C_1 S^2 + \left(C_2 \left(R_1 + R_2 \right) + R_1 C_1 \left(1 - K \right) \right) S + 1}$$

for $K = 1$

For $\omega = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$

$\frac{2\zeta}{\omega} = C_2 \left(R_1 + R_2\right)$ or $\zeta = \frac{C_2 \left(R_1 + R_2\right)\omega}{2}$

$C_1 = \frac{R_1 + R_2}{R_1 R_2} \left(\frac{1}{2\zeta\omega_N}\right)$, $C_2 = \frac{2\zeta}{(R_1 + R_2)\omega_N}$

242 Hz $\zeta = 0.483$ 232 Hz $\zeta = 0.938$

$$C_1 = \frac{5100 + 5100}{(5100)^2} \times \frac{1}{2 \times 0.483 \times 2\pi \times 242}$$

$$= \frac{2}{5100} \times \frac{1}{4\pi \times 0.483 \times 242}$$

$$= \frac{1}{375 \times 10^4}$$

$$= \frac{10^{-6}}{3.75} = 0.267\ \mu F$$

$$C_1 = \frac{5100 + 5100}{(5100)^2} \times \frac{1}{2 \times 0.938 \times 2\pi \times 232}$$

$$= \frac{2}{5100} \times \frac{1}{4\pi \times 0.938 \times 232}$$

$$= \frac{1}{699 \times 10^4}$$

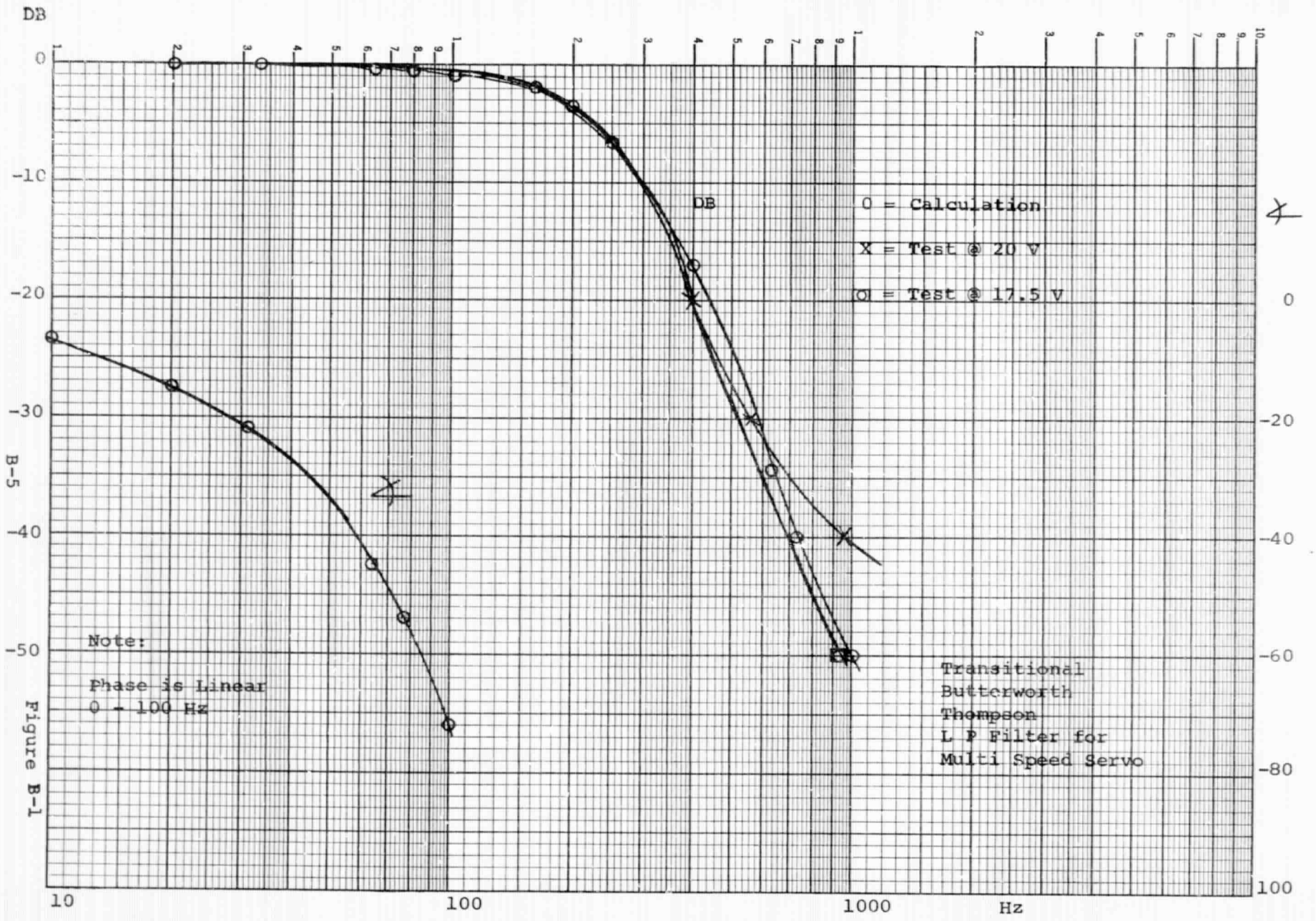
$$= \frac{10^{-6}}{6.99} = 0.143\ \mu F$$

$$C_2 = \frac{2 \times 0.483}{2 \times 5100 \times 2\pi \times 242} \qquad C_2 = \frac{2 \times 0.938}{2 \times 5100 \times 2\pi \times 232}$$

$$= \frac{0.966}{1.02 \times 10^4 \times 484\pi} = \frac{10^{-6}}{4.84} \qquad = \frac{1.876}{1.02 \times 10^4 \times 464\pi}$$

$$= 0.0623\ \mu F \qquad = 0.126\ \mu F$$

Test results are compared with calculations in figure B-1.


DB
0
-10
-20
-30
-40
-50
DB
O = Calculation
X = Test @ 20 V
□ = Test @ 17.5 V
Note:
Phase is Linear
0 - 100 Hz
Transitional
Butterworth
Thompson
L P Filter for
Multi Speed Servo
0
-20
-40
-60
-80
-100
10
100
1000
Hz

B-5

Figure B-1